On the Use of Current Control Scheme for Switched-Capacitor DC/DC Converters

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Abstract—This paper presents an investigation into the use of a current control scheme (CCS) and a comparison with a classical switching scheme for switched-capacitor (SC) step-down dc/dc converters. With the CCS, capacitors are charged with near-constant current, controlled by the gate–source voltage of MOSFET’s. By paralleling two SC cells, the converter input current becomes continuous, resulting in much reduced conducted electromagnetic interference with other circuits fed by the same power supply. All MOSFET’s are operated for half of the switching period, in order to improve the regulation capability. Static and dynamic behaviors of the converter with the CCS are predicted and confirmed in an experimental 36-W 12-V/9-V prototype.

Index Terms—DC/DC power conversion, switched capacitor circuits, switched circuits, switched-mode power supplies.

I. INTRODUCTION

In recent years, switched-capacitor (SC)-based converters, which comprise primarily switches and capacitors, have been proposed [1]–[6] and commercialized. They have the advantage of eliminating inductive element in power conversion. Thus, possibilities of integrated circuit (IC) fabrication and high power density are much more promising. Starting from an original idea of using a basic SC cell in digital filter design [7] for power conversion, many methodologies of operating the switches and the capacitors, and the control schemes have been proposed. Each capacitor is basically going through a charging process from the supply and/or other capacitors, and a discharging process to the load and/or other capacitors, periodically. However, the voltage conversion ratio of the converters in [1] and [2] and those cited as commercially available1 is dependent on the circuit structure, having a drawback of weak regulation capability.

In order to improve voltage regulation, an on-resistance control scheme has been used in [4]. The MOSFET is driven into the triode region during the charging phase, forming a voltage-controlled resistor. In [5] and [6], the charging time of the capacitors is controlled by a pulsewidth modulation (PWM) control scheme, providing adjustable voltage conversion ratio. Nevertheless, all of the above converters have the common drawbacks of: 1) drawing pulsating input current that causes conducted electromagnetic interference (EMI) with the supply network [8] and 2) having high current stress on the switching devices in charging the capacitors.

In order to reduce the current stress on switches, use of the current control scheme (CCS) in the charging process has been proposed in [9] and [10], which has the advantageous feature of suppressing current spikes. MOSFET’s are driven into the saturation region during the charging process. In [9], the charging interval is determined by a duty-cycle control and the current magnitude is adjusted by the gate–source voltage of the MOSFET’s. Nevertheless, the converter input current is still discontinuous. Recently, an SC dc/dc boost converter cell that features continuous input current and good regulation capability has been reported in [10]. All capacitors are charged with constant current for a fixed duration in every switching cycle.

Based on [10], a CCS, which is specially designed for a step-down converter, is presented in this paper. The concept of energy transfer is achieved by paralleling the input and output of two converter cells and operating them in antiphase. Each converter cell features constant charging current, resulting in a continuous input current waveform. The voltage conversion ratio is determined by the gate–source voltage applying to a MOSFET in each cell. The principle of operation and a comparison with a classical switching scheme (CSS) are given in Section II. Static and small-signal dynamic characteristics of the converter are derived in Section III. In Section IV, theoretical predictions are verified with experimental measurements of a 36-W 12-V/9-V prototype. The conclusions are given in Section V.

II. PRINCIPLES OF OPERATION

A typical SC cell is shown in Fig. 1, including a capacitor $C$ with equivalent series resistance (ESR) $r_C$, and two MOSFET’s $S$ and $Q_S$. It forms a fundamental building unit for the step-down converter. The basic idea is that the capacitor is going through a charging process from the supply (i.e., $v_{in}$) and/or other capacitors, and a discharging process to the load.

Fig. 1. Typical SC converter cell.
(i.e., \( R_L \)) and/or other capacitors, periodically. In the CSS, both \( S \) and \( QS \) are operated as static switches. Voltage regulation can be achieved by adjusting either the switching frequency in [3] or the capacitor charging duration in [5] and [6]. In the proposed CCS, \( S \) is still operated as a static switch, but \( QS \) is operated between saturation and cutoff regions. For a MOSFET operating in the saturation region, its gate–source voltage \( V_{GS} \) and its drain current \( i_D \) can be related by a large-signal model [11]

\[
i_D = K_1(v_{GS} - V_T)^2, \quad K_1 = \frac{1}{2} k_1 k_2
\]

where \( k_1 \) is the process transconductance parameter, which is determined by the fabrication technology, \( k_2 \) and \( V_T \) are the aspect ratio and the threshold voltage of the MOSFET channel, respectively. The small-signal variation of \( i_D \) with respect to changes of \( V_{GS} \) can be studied by introducing perturbations into (1) with \( i_D = I_D + \dot{i}_D \) and \( V_{GS} = V_{GS} + \dot{v}_{GS} \). Thus,

\[
I_D = K_1(V_{GS} - V_T)^2 \tag{2}
\]

and

\[
\dot{i}_D = K_1[2\dot{v}_{GS}(V_{GS} - V_T) + \dot{i}_{GS}^2] \approx K_2 \dot{v}_{GS}
K_2 = 2K_1(V_{GS} - V_T) \tag{3}
\]

where \( I_D \) and \( V_{GS} \) are the steady-state drain current and gate–source voltage, respectively.

Hence, a saturated MOSFET behaves as an ideal current source, whose value is controlled by \( v_{GS} \) according to the square-law relationship in (2).

Within a switching cycle of period \( T_S \), \( S \) and \( QS \) are operated alternately for the same duration of \( T_S/2 \). The cell is switched between two topologies, which are shown in Fig. 2. The first topology is the capacitor charging phase. \( QS \) is opened and \( S \) is closed. \( C \) is charged by \( v_{in} \) with constant current \( I_{th} \), which is controlled by the gate–source voltage of \( QS \) [see (2)]. This gives a linear trajectory on the capacitor voltage. The final capacitor voltage will be slightly higher than the desired output voltage, in order to compensate the parasitic voltage drop in the second topology. The second topology is the capacitor discharging phase. \( QS \) is open and \( S \) is closed. \( C \) is disconnected from \( v_{in} \) and/or other capacitors and supplies to \( R_L \) and/or other capacitors.

Similarly to [5], [6], and [10], a step-down dc/dc converter is realized by paralleling two cells, namely, cell 1 and cell 2 in Fig. 3(a), and operating them in antiphase. Although the schematics of the converter are the same as the one in [5], the switching scheme is improved. Instead of having four topologies, the converter is only switched between two topologies, namely, Topology 1 and Topology 2, with the CCS.

In Topology 1 [Fig. 3(b)], cell 1 is in charging phase and cell 2 is in discharging phase. \( C_1 \) is charged linearly by \( I_{th} \) to a voltage slightly higher than the output voltage \( v_{out} \), in order to compensate parasitic voltage drop. \( C_2 \) supplies \( R_L \) through \( S_2 \). In Topology 2 [Fig. 3(c)], the operation is similar to Topology 1, except the operating phases of cell 1 and cell 2 are interchanged. That is, cell 1 is in discharging phase and cell 2 is in charging phase.
Comparing to the CSS, the CCS exhibits the following advantages and phenomena.

A. Continuous Input Current

The capacitor charging current in the CSS is pulsating—causing high current stress on the switching devices. The input current waveform of the converters using the CSS in [2] and [3] is shown in Fig. 4(a) and that using the CSS in [5] and [6] is shown in Fig. 4(b). These input current waveforms actually correspond to the charging current of the capacitors [as in Fig. 2(a)]. It is important to note that these currents are not actively controlled. Both of them are in exponential decay with an initial peak current which is dependent on the input voltage, the parasitic resistance of the charging circuit, and the capacitor voltage after the discharging phase. Comparing Fig. 4(a) and (b), the capacitors in [2] and [3] and those cited as commercially available are fully charged, while the ones in [5] and [6] are partially charged during the charging phase. In both cases, the charging current \( i_{\text{CSS}} \) in one switching cycle \( T_s \) can be expressed as

\[
i_{\text{CSS}}(t) = I_{\text{CSS,max}} e^{-(t/T_s)}
\]

where \( \tau \) is the time constant of the charging circuit. Time variable \( t \) is defined between 0 and \( T_s \) for the waveform in Fig. 4(a) and is defined between 0 and \( t_1 \) for the waveform in Fig. 4(b). As both of the waveforms are periodic, each one can be expressed in a form of an exponential Fourier series as

\[
i_{\text{CSS}}(t) = \sum_{n=-\infty}^{\infty} F_n e^{j \omega_0 n t}
\]

where

\[
F_n = \begin{cases} 
\frac{I_{\text{CSS,max}}}{T_s} \frac{1 - e^{-(T_s/\tau)}}{(1/\tau)^2 + n^2 \omega_0^2}, & \text{for the waveform in Fig. 4(a)} \\
\frac{I_{\text{CSS,max}}}{T_s} \frac{1 - 2e^{-(t_1/\tau)} + e^{-(2T_s/\tau)}}{(1/\tau)^2 + n^2 \omega_0^2}, & \text{for the waveform in Fig. 4(b)}
\end{cases}
\]

\[\omega_0 = \frac{2\pi}{T_s}.
\]

Thus, the frequency spectrum of \( i_{\text{CSS}} \) covers a wide range of frequencies in both cases. With the CCS, the charging current of each capacitor is a constant of \( I_{dc} \). As the two cells are connected in parallel, the converter input current theoretically becomes a constant value of \( I_{dc} \). The input current waveform is illustrated in Fig. 4(c). Hence, the frequency spectrum of the input current theoretically contains dc component only without harmonics.

In addition, with the same voltage variation on a capacitor in one switching cycle, the charge transferred from the source to the capacitor is independent of the charging scheme. That is,

\[
I_{dc} T_s = \int_0^{T_s} i_{\text{CSS}}(t) \, dt
\]

\[\Rightarrow \frac{I_{dc}}{I_{\text{CSS,max}}} = \begin{cases} 
\frac{\tau}{T_s} (1 - e^{-(T_s/\tau)}), & \text{for the waveform in Fig. 4(a)} \\
\frac{\tau}{T_s} (1 - e^{-(t_1/\tau)}), & \text{for the waveform in Fig. 4(b)}
\end{cases}
\]

As \( \tau \ll T_s, I_{dc} \ll I_{\text{CSS,max}} \). Thus, the peak current ratio \( I_{dc}/I_{\text{CSS,max}} \) in (6) shows that the current stress on the switching elements with the CCS is much lower than that of the CSS. Therefore, the CCS can improve the input current waveform, lower current stress on switching devices, and reduce conducted EMI [8].

B. Improved Regulation Capability

Compared to the converters having adjustable voltage conversion ratio, such as the ones in [5] and [6], the charging time of the capacitors is controlled by PWM technique [i.e., adjusting \( t_1 \) in Fig. 4(b)]. Under the steady-state condition, the average
Mathematically, in order to investigate the regulation capability of the converters using PWM technique, a normalized discharging current with respect to the duty cycle of the switches (i.e., \( t_1/T_S \)) is defined as:

\[
I_N = \left( \frac{I_{CSS}}{I_{CSS\text{max}}} \right) \left( 1 - e^{-\left( t_1/T_S \right)} \right)
\]  

(7)

where \( I_{CSS\text{max}} \) is the maximum capacitor discharging current, which is taken as the base value. As shown in Fig. 2(b), the discharging current directly correlates to the load current. \( I_N \) can be considered as the normalized output current. For different \( \tau/T_S \) ratios, the relationships between \( I_N \) and \( t_1/T_S \) are shown in Fig. 5. It can be observed that the conduction time will be short and the corresponding gating pulsewidth will be narrow at light load or at low output voltage condition, especially for small \( \tau/T_S \) ratios. For example, if \( \tau/T_S = 0.2 \) and \( t_1/T_S = 0.1 \) (10%), only a value of 0.4 for \( I_N \) can be achieved. In order to achieve a lower value of \( I_N \), it is necessary to make \( t_1 \) smaller. However, such PWM control becomes practically hard to implement if \( t_1 \) is too narrow. Conversely, with the CCS, the duty cycle of all switching devices is fixed at 0.5. Thus, its regulation capability is improved since the control circuit is only required to provide a desired gate–source voltage to control the drain current of \( QS_1 \) and \( QS_2 \) with fixed duty cycle of 0.5.

C. Similar Conversion Efficiency as CSS

The major difference between the CSS and CCS is in the capacitor charging process. It can be shown that the energy loss \( E_{loss} \) in charging \( C \) from an initial voltage \( v_{C_i} \) to a final voltage \( v_{C_f} \) in Fig. 2(a) is:

\[
E_{loss} = \frac{1}{2} C \left[ (v_{in} - v_{C_i})^2 - (v_{in} - v_{C_f})^2 \right].
\]  

(9)

\( E_{loss} \) is independent of the switching scheme. Thus, CCS gives similar performance index as the previous converters, but presents much better performance characteristics, as discussed in Sections II-A and II-B.

III. ANALYSIS OF THE CONVERTER

By applying the state-space averaging technique and assuming \( C_1 = C_2 = C \), a state-space representation of the converter in Fig. 3(a) can be described as follows:

\[
\dot{x} = A_{av}x + B_{av}I_{ch}
\]

\[
v_{out} = C_{av}x
\]

(10)

where

\[
x = [v_{C_1} \ v_{C_2} \ v_{C_0}]^T
\]

\[
A_{av} = \begin{bmatrix}
-R_L + r_{C_2}/2C & 0 & R_L/2C \\
0 & -R_L + r_{C_0}/2C & R_L/2C \\
R_L/2C & R_L/2C & -R_L + r_a/\beta
\end{bmatrix}
\]

\[
B_{av} = \begin{bmatrix}
1/2C \\
1/2C \\
0
\end{bmatrix}^T
\]

\[
C_{av} = \begin{bmatrix}
r_Cr_L \\
R_Cr_L/2\beta \\
r_a
\end{bmatrix}
\]

\[
\beta = r_S + r_C
\]

A. Steady-State Characteristics

By putting \( \dot{x} = 0 \) into (10) and using (2), the averaged output voltage \( v_{out} \) is:

\[
v_{out} = C_{av}(V_{GS} - V_T)^2
\]

(11)

\( V_{GS} \) is generally derived from the feedback circuit in a regulator, after comparing \( v_{out} \) with a reference voltage. Although \( v_{out} \) has a nonlinear relationship with \( V_{GS} \), \( V_{GS} \) is relatively constant in every cycle because the variation of the output of the feedback network is usually slow as compared to the switching frequency. Based on (2), a stable \( V_{GS} \) will offer a relatively constant drain current and, hence, the output voltage. As shown in Fig. 3, provided that all \( QS \)'s are operated in saturation mode, the charging current \( I_{ch} \) is independent of the input voltage \( v_{in} \). Nevertheless, the maximum value of \( I_{ch} \) is dependent on \( v_{in} \) when \( QS \) is at the verge of triode mode. The converter will lose the regulation because all \( QS \)'s are fully turned on during the charging phase. The operation will become similar to the converters in [2] and [3] and those cited as commercially available.

Mathematically, by using (10), the averaged steady-state capacitor voltages \( V_{C_1} \) and \( V_{C_2} \) are:

\[
V_{C_1} = V_{C_2} = \begin{bmatrix} 1 & 0 \end{bmatrix} [(-A_{in}^{-1}B_{av})I_{ch} = R_LI_{ch} = R_LK_1(V_{GS} - V_T)^2.]
\]  

(12)

During the charging phase,

\[
I_{ch} < \frac{V_{in} - V_{C_1}}{r_{C_1} + R_{QS}}
\]

\[
\Rightarrow R_L > \frac{V_{out}(r_{QS} + 2r_C + r_S)}{v_{in} - V_{out}}
\]

(13)

where \( r_{QS} \) is the on resistance of \( QS \). Thus, (13) gives the minimum value of \( R_L \) such that the converter can still provide...
voltage regulation. It can be observed that the load range depends on the parasitic resistance of the components, input, and output voltages.

B. Conversion Efficiency

Based on (11), the output current $I_{\text{OUT}}$ can be shown to be

$$I_{\text{OUT}} = \frac{V_{\text{OUT}}}{R_L}$$  \hspace{1cm} (14a)

$$\Rightarrow I_{\text{OUT}} = I_{ch}.$$  \hspace{1cm} (14b)

Thus, the conversion efficiency $\eta$ can be shown to be

$$\eta = \frac{\text{Output Power}}{\text{Input Power}} = \frac{V_{\text{OUT}} I_{\text{OUT}}}{V_{\text{IN}} I_{ch}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}}. \hspace{1cm} (15)$$

If the difference between $V_{\text{IN}}$ and $V_{\text{OUT}}$ decreases, $\eta$ increases. Particularly, $\eta$ is equal to one when $V_{\text{OUT}} = V_{\text{IN}}$, which is the case of minimum energy loss (9). With a multistage SC cell configuration as in [6], high conversion efficiency can be obtained for a bigger difference between $V_{\text{IN}}$ and $V_{\text{OUT}}$.

C. Small-Signal Dynamic Characteristics

By using (3) and (10), the small-signal control-to-output transfer function can be shown to be

$$G_{OC}(s) = \frac{\tilde{i}_{\text{OUT}}(s)}{\tilde{i}_{\text{GS}}(s)} = K_2C_{ao}(sI - A_{av})^{-1}B_{av}$$

$$= \frac{K_2R_L(1 + C_{ao}C_{bo}s)}{1 + a_1s + a_0s^2} \hspace{1cm} (16)$$

where $a_0 = 2C_{ao}C_{bo}$ and $a_1 = 2C_{bo}(r_o + R_L) + C_{ao}(r_{ao} + R_L)$.

As shown in Fig. 3, provided that $QS_1$ and $QS_2$ are operated in the saturated region, the charging current of the capacitors can be kept at $I_{ch}$, which is independent of $V_{\text{IN}}$. Hence, based on (11), $V_{\text{OUT}}$ is independent of $V_{\text{IN}}$. Thus, the input-to-output transfer function theoretically equals zero in the normal operation.

IV. Prototype

A 36-W 12-V/9-V step-down regulator has been realized in the laboratory. It is shown in Fig. 6. The values of the elements are $C_a = C_1 = C_2 = 47 \, \mu F$ (multilayered ceramic type) with ESR 0.01 $\Omega$. Toshiba MOSFET's 2SJ334 and 2SK942 were used for all switches $S$ and all switches $QS$, respectively. The on-resistance of 2SJ334 is 29 m$\Omega$. $K_1$ of 2SK942 at the rated operation is approximately 5.6 $A/V^2$. The switching frequency is 180 kHz. Fig. 7(a) shows the experimental output voltage waveform and input current. It can be observed that the input current is near continuous. Fig. 7(b) shows the current waveform of one
Inductorless dc-to-dc converter with high power density, a step-down dc/dc converter. It exhibits all positive characteristics, and the output power is further increased. The converter can regulate the output voltage at 9 V when the output power is less than 45 W. Loss of regulation occurs when the output power increases. The results of the output voltage of the converter with respect to the output power are shown in Fig. 10. It can be seen that the converter with theoretical and experimental control-to-output transfer characteristics is shown in Fig. 9, showing close agreement with each other. Experimental results of the output voltage of the converter with respect to the output power are shown in Fig. 10. It can be seen that the converter can regulate the output voltage at 9 V when the output power is less than 45 W. Loss of regulation occurs when the output power is further increased.

V. CONCLUSIONS

This paper has presented a CCS specially designed for a SC step-down dc/dc converter. It exhibits all positive characteristics of previous SC converters and has the extra advantages of continuous input current and good regulation capability. It also provides adjustable voltage conversion ratio, which is independent of circuit structure. A 12-V/9-V step-down converter prototype has been built at a nominal output power of 36 W. Further research will be directed toward the development of the CCS for multistage SC step-down converters.

REFERENCES


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