Computer Science 141: Computing Hardware

Spring 2020

1 Outline

The main emphasis of this course is on the basic concepts of digital computing hardware and fundamental digital design principles and practices for computer systems. This course focuses on digital devices and systems, and it complements ES 152, which focuses on devices and systems that use analog electronics. Topics include: combinational and sequential logic; computer architecture; machine code; and altogether the infrastructure and computational framework composing a MIPS processor.

An integral component of this course will be a sequence of hands-on hardware projects where you will build digital circuits using logic gates and make use of some common software packages for Computer-Aided Design (CAD) and FPGA-based prototyping. Through these projects, you will learn how to design, test, and construct complex hardware systems that interact with the real world. The hardware projects will start with simple logic and end with you building a small multicycle processor implemented in hardware on an FPGA board.

There is overlap between CS 141 and Physics 123/ES 153. If you have questions about which course you should take, please feel free to see Professor Reddi. CS 141 is more focused on computer architecture and machine organization while Physics 123/ES 153 addresses the design of practical analog and digital circuits. CS 141 is good preparation for students interested in computer architecture (CS 146/246), VLSI (CS 148/248), and edge computing (CS 249r).

2 Administrative Information

Lectures:	Monday, Wednesday 1:30–2:45pm in Maxwell Dworkin G119
Instructor:	Professor Vijay Janapa Reddi (`vj@eecs.harvard.edu`) 147 Maxwell Dworkin
Course Admin:	Carol Harlow (`harlow@seas.harvard.edu`) 343 Maxwell Dworkin, 496-1440
Teaching Fellows:	Zachary Yedidia (`zyedidia@college.harvard.edu`) Jon Cruz (`jcruz@g.harvard.edu`) Dhilan Ramaprasad (`dhilanramaprasad@college.harvard.edu`) Gayatri Balasubramanian (`gayatrib@college.harvard.edu`)

Regular office hours and lab-specific office hours will be posted on the course website.

3 Course Prerequisites

CS 50 is the formal prerequisite for this course. *CS 61* is helpful preparation but not required. An understanding of binary numbers and some knowledge of basic electronics are helpful but not necessary. If you have any questions about your preparation, please contact Professor Reddi directly.

4 Course Requirements

4.1 Lectures

While attendance at lecture is not required, it is encouraged. In addition, while lecture slides and additional notes will be provided, they are not complete nor guaranteed to be correct nor a substitute for attending lecture.

4.2 Sections

We will arrange *weekly* sections that will be led by one (or more) of the TFs. The section will discuss additional material especially regarding SystemVerilog and FPGA development, but also to review lecture material. Again, attendance is strongly encouraged, as the material will be helpful for weekly assignments and exams.

4.3 Regular assignments

Assignments consisting of a problem set and associated hardware project will be assigned most weeks of the class.

4.3.1 Problem sets

Problem sets are due at the **beginning** of class, unless otherwise noted. Problem sets should be done individually.

Electronic submission rules: Problem sets must be submitted electronically using Canvas. This course requires many circuit diagrams, which past students have preferred to draw by hand. If you submit electronically, you **MUST** obey the following rules. Failure to comply may result in you receiving a zero on that assignment.

- Attach your homework as a single PDF file. Do not attach multiple files.
- Solutions must be legible. Problems that cannot be read due to illegible handwriting or low quality scans will receive a score of zero.

Please see the *policy on late assignments* below.

4.3.2 Hardware projects

The course will include hardware projects that you will work on with a partner.

The projects will primarily be done at home, and you will have the opportunity to ask questions at several project office hours arranged by the teaching staff.

Projects will be due Friday of each week and will be demo'ed at a session arranged by the teaching staff. A project pair will turn in a single copy of the project. It will be up to you and your partner to distribute work appropriately, but everyone is responsible for understanding the entire project. During the demo, the TF will ask both of you individual questions about the project, and grades will be assigned separately based on your individual responses to the question. Do not let the first few projects lull you into a false sense of security; the projects increase in complexity significantly in later weeks. You must complete all of the project assignments (please see the *policy on late assignments* below).

4.4 Policy on late assignments

Every student will get 2 late days for problem sets and 2 late days for projects.

4.5 Policy on cooperation and academic integrity

Discussion and the exchange of ideas are essential to doing academic work. For assignments in this course, you are encouraged to consult with your classmates as you work on problem sets. However, after discussions with peers (or course instructional staff such as tutors, TF/TAs, course assistants),

make sure that you can work through the problem yourself and ensure that any answers you submit for evaluation are the result of your own efforts. For problem sets and projects students are permitted to ask classmates and others for conceptual help so long as that help does not reduce to another doing your work for you. Collaboration on the course's final project is permitted to the extent prescribed by its specification. In addition, you must cite any books, articles, websites, lectures, etc that have helped you with your work using appropriate citation practices. Similarly, you must list the names of students with whom you have collaborated on problem sets if you feel there may be any concern of overlap.

If in doubt as to whether some act is reasonable, do not commit it until you solicit and receive approval in writing from the course staff. Acts considered not reasonable are handled harshly. If the course refers some matter to the Administrative Board and the outcome is Admonish, Probation, Requirement to Withdraw, or Recommendation to Dismiss, the course reserves the right to impose local sanctions on top of that outcome. If you commit some act that is not reasonable but bring it to the attention of the course staff within 48 hours, the course may impose local sanctions, but the course will not refer the matter to the Administrative Board except in cases of repeated acts.

Harvard College Honor Code

Members of the Harvard College community commit themselves to producing academic work of integrity – that is, work that adheres to the scholarly and intellectual standards of accurate attribution of sources, appropriate collection and use of data, and transparent acknowledgement of the contribution of others to their ideas, discoveries, interpretations, and conclusions. Cheating on exams or problem sets, plagiarizing or misrepresenting the ideas or language of someone else as one's own, falsifying data, or any other instance of academic dishonesty violates the standards of our community, as well as the standards of the wider world of learning and affairs.

4.6 Diversity and Inclusion

In an ideal world, science would be objective. However, much of science is subjective and is historically built on a small subset of privileged voices. We acknowledge that it is possible that there may be both overt and covert biases in the material due to the lens with which it was written, even though the material is primarily of a scientific nature. Since integrating a diverse set of experiences is important for a more comprehensive understanding of science please contact the course staff (in person or electronically) or submit anonymous feedback if you have any suggestions to improve the quality of the course materials.

We would like to create a learning environment that supports diversity of thoughts, perspectives, and experiences, and honors your identities. If you have a name and/or set of pronouns that differ from those that appear in your official records, please let us know!

If you feel like your performance in the class is being impacted by your experiences outside of class, please don't hesitate to contact us. If you prefer to speak with someone outside of the course, the SEAS Director of Diversity, Inclusion and Belonging is an excellent resource.

So that the course staff has enough time to implement accommodations, students needing academic adjustments or accommodations because of a documented disability must present their Faculty Letter from the Accessible Education Office (AEO) and speak with the course staff by the end of the second week of the term. All discussions will remain confidential, although the course staff may contact the AEO to discuss appropriate implementation.

4.7 Exams

There will be an in-class midterm exam (tentatively scheduled for Wednesday March 4th) and a final exam (scheduled for May 11th at 2pm).

5 Grading

Your final grade will be based roughly on the following weighting of your course work:

20%	Midterm exam
20%	Final exam
20%	Problem sets
40%	Hardware projects

6 Reading

6.1 Required text

David M. Harris and Sarah L. Harris. *Digital Design and Computer Architecture.* Morgan Kaufmann.

6.2 Recommended texts

Pong P. Chu. *FPGA Prototyping by SystemVerilog Examples.* Wiley.

John F. Wakerly. *Digital Design Principles and Practices.* Prentice Hall.

David A. Patterson and John L. Hennessy. *Computer Organization & Design: The Hardware/Software Interface.* Morgan Kauffman.

Randy Katz. *Contemporary Logic Design.* Benjamin/Cummings.

7 Educational software

Software will be provided to compile designs onto the FPGA prototype boards. In particular we will be using Xilinx Vivado from inside a Linux virtual machine. Installation instructions will be provided.