Harvard John A. Paulson School of Engineering and Applied Sciences

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RESEARCH EXPERTISE

Research Areas: Machine Learning Systems, Runtime Systems; Compilers; Computer Architecture
Research Domains: Machine Learning; Mobile Computing; Autonomous Machines/Vehicles; Robotics

EDUCATION

Harvard University	Computer Science	Ph.D.	2010
University of Colorado—Boulder	Electrical and Computer Engineering	M.S.	2006
Santa Clara University	Computer Engineering	B.S.	2003

CURRENT AND PREVIOUS ACADEMIC POSITIONS

Harvard University	Associate Professor	Jan 2019 – Present
The University of Texas at Austin	Adjunct Associate Professor	Sep 2018 – Present
The University of Texas at Austin	Associate Professor	Aug 2017 – Aug 2018
The University of Texas at Austin	Assistant Professor	Aug 2011 – Jul 2017

OTHER PROFESSIONAL INDUSTRY EXPERIENCE

Google (Tensor Flow Ecosystem)	Visiting Researcher	Mar 2020 - Dec 2021
Facebook (AR Silicon Team)	Visiting Researcher	Jan 2019 – Dec 2019
Google (gChips)	Visiting Researcher	Mar 2017 – Dec 2018
Intel	Consultant	Jun 2015 – Dec 2016
Advanced Micro Devices (AMD)	Consultant	Feb 2015 – Dec 2016
Intel	Consultant	Jun 2014 – Aug 2014
Advanced Micro Devices (AMD)	Senior Design Engineer	Jul 2010 – Jul 2011
Microsoft Research	Research Intern	Mar 2009 – Jun 2009
VMware	Research Intern	Jan 2007 – Mar 2009
Intel	Research Intern	Apr 2003 – Dec 2006

HONORS AND AWARDS

- MLPerf Inference selected for inclusion in ISCA@50 25-Year Retrospective: 1996-2020, 2023.
- Top Picks in Computer Architecture (Honorable Mention), *IEEE Micro*, 2023.
- Top Picks in Computer Architecture (Honorable Mention), *IEEE Micro*, 2022.
- BenchCouncil Rising Star Award, *International Open Benchmark Council*, 2021.
- Deploying TinyML on HarvardX/edX - 100 Most Popular Free Online Courses, *ClassCentral*, 2021.
- Best Course in AI: Tiny Machine Learning (TinyML) on HarvardX/edX, *CogX Awards,* 2021.
- Top Picks in Computer Architecture, *IEEE Micro*, 2021.
- Best of Computer Architecture Letters (CAL), Editorial Board of IEEE CAL, 2021.
- Programming Languages Software Award, *ACM SIGPLAN,* 2020.
- Best Research Paper Award, *Design Automation Conference (DAC), 2020.*
- Google Faculty Research Award, *Google*, 2012, 2013, 2015, 2017, 2020.
- Best Paper Nominee, IEEE *Intl. Symp. on Performance Analysis of Systems and Software (ISPASS)*, 2019.
- HPCA Hall of Fame, *IEEE/ACM Intl Symp. on High-Performance Computer Architecture (HPCA)*, 2019.
- MICRO Hall of Fame, *IEEE/ACM International Symp. on Microarchitecture (MICRO)*, 2018.
- ACM SIGARCH CS TCCA Outstanding Dissertation Award (Advisee: Yuhao Zhu), *SIGARCH*, 2018.
- Top Picks in Computer Architecture, *IEEE Micro*, 2017.
- Best Paper Nominee, *Design Automation Conference (DAC)*, 2017.

- IEEE TCCA Young Computer Architect Award, *IEEE Computer Society*, 2016.
- Top Picks in Computer Architecture (Honorable Mention), *IEEE Micro*, 2016.
- Gilbreth Lectureship Honor, *National Academy of Engineering (NAE)*, 2016.
- Most Influential PLDI Paper Award, *ACM SIGPLAN*, 2015.
- Best of Computer Architecture Letters (CAL) Award, Editorial Board of IEEE CAL, 2014.
- Best Paper Nominee, *IEEE Intl. Symp. on Low Power Electronics and Design (ISLPED)*, 2014.
- Indo-American Frontiers of Engineering, *National Academy of Engineering (NAE)*, 2014.
- Intel Early Career Honor Award, *Intel*, 2013.
- Top Picks in Computer Architecture, *IEEE Micro*, 2011.
- Top Picks in Computer Architecture, *IEEE Micro*, 2010.
- Best Paper Award, *Intl. Symp. on High-Performance Computer Architecture (HPCA)*, 2009.
- John A. and Elizabeth S. Armstrong Fellowship, *Harvard University*, 2008.
- Best Student Presentation, *Intl. Symp. on Code Generation and Optimization (CGO)*, 2007.
- Top Picks in Computer Architecture, *IEEE Micro*, 2006.
- Best Paper Award, *Intl. Symp. on Microarchitecture (MICRO)*, 2005.
- Faculty Recognition for Technical Excellence, *Santa Clara University*, 2003.
- Outstanding Undergraduate (Honorable), *Computing Research Association (CRA)*, 2003.

MEMBERSHIPS IN PROFESSIONAL AND HONORARY SOCIETIES

Member: Institute of Electrical and Electronics Engineers (IEEE)
Member: Association for Computing Machinery (ACM)

UNIVERSITY COMMITTEE ASSIGNMENTS

Harvard SEAS	Member, Engineering Sciences Committee on Higher Degrees	2023-2024
	Member, Generative AI Steering Committee	2023
	Member, Quantum Faculty Recruiting Committee	2020
	Member, Robotics Faculty Recruiting Committee	2020
	Graduate Student Admissions Committee	2019 - Present
UT Austin	Member, Faculty Recruiting Committee	2016
	Member, Faculty Recruiting Committee	2015
	Member, Technology in Teaching	2014
	Member, Faculty Recruiting Committee	2013
	Graduate Student Admissions Committee	2011 - 2016

PROFESSIONAL SOCIETY AND MAJOR GOVERNMENTAL COMMITTEES

- MLCommons (http://mlcommons.org)
  - Vice-Chair (on the Board of Directors) (2019 – Present)
  - o Vice President (2019 – Present)
  - MLCommons Research Co-Chair (2019 – Present)
- MLPerf (http://mlperf.org)
  - MLPerf Tiny Co-Chair (2019 – 2020)
  - MLPerf Inference Co-Chair (2018 – 2020)
- International Roadmap for Devices and Systems (IRDS™ 2020 – Present)
  - Applications Benchmarking International Focus Team (AI Team)
- Associate Editor, SIGARCH Blog (http://sigarch.org/blog/) (2017 – 2020)
- General Chair
  - Tiny Machine Learning Research Symposium (TinyML 2022)

  - Intl. Symp. on Code Generation and Optimization (CGO 2017)
- Program Committee Chair
  - Tiny Machine Learning Research Symposium (TinyML 2021)
  - IEEE Intl. Symp. on Workload Characterization (IISWC 2019)
  - Intl. Symp. on Code Generation and Optimization (CGO 2014)
- Program Committee:
  - High-Performance Computer Architecture (HPCA-30)
  - Neural Information Processing Systems (NeurIPS 2022)
  - Intl. Symp. on Computer Architecture (ISCA 2014, 2018erc, 2020, 2021, 2022, 2023)
  - Machine Learning Systems (MLSys 2021)
  - Microarchitecture (MICRO 2013, 2014, 2018, 2020)
  - Design Automation Conference (DAC 2020)
  - IEEE Micro Top Picks (2016, 2018, 2019, 2021)
  - Code Generation and Optimization (CGO 2013, 2014, 2019, 2021)
  - Arch. Support for Programming Languages and Operating Systems (ASPLOS 2018, 2021)
  - High Performance Computer Architecture (HPCA 2012, 2014, 2015, 2017erc, 2023)
  - Principles and Practice of Parallel Computing (PPoPP 2013, 2015)
  - Parallel Architectures and Compilation Techniques (PACT 2013)
  - Workload Characterization (IISWC 2012, 2013, 2016, 2018)
  - Parallel & Distributed Processing (IPDPS 2012)
  - Performance Analysis of Systems and Software (ISPASS 2012)
- ACM SRC Chair
  - Intl. Symp. Parallel Architectures and Compilation Techniques (PACT 2017)
- Finance Chair
  - Intl. Symp. on Code Generation and Optimization (CGO 2015)
- Steering Committee
  - Intl. Symp. on Code Generation and Optimization (CGO) (2014 – Present)
- Guest Editor
  - IEEE Micro Special Issue on Reliability-Aware Microarchitecture Design (2013),
  - IEEE Micro Special Issue on Internet of Things (2016)
- Local Arrangements Chair
  - Intl. Symp. on Performance Analysis of Systems and Software (ISPASS 2013)
  - Workshop on Silicon Errors in Logic - System Effects (SELSE 2015, 2016)
- Publications Chair
  - Intl. Symp. on Workload Characterization (IISWC 2013)
- Organizer
  - Data-centric Machine Learning Research (DMLR) Workshop (ICML 2023)
  - Workshop on Cognitive Edge Computing (CogEdge 2016-2017)
  - Tutorial on Tools for Mobile Computer Architecture (MobiTools 2016)
  - Tutorial on Simulation and Analysis Engine (ISCA 2016, ASPLOS 2016, HPCA 2016, ICS 2016, IISWC 2015, ISPASS 2015)
  - Workshop on Resilient Architectures (WRA 2013–2010)

COMMUNITY ACTIVITIES

- Hands-on Computer Science (HaCS) for Austin Independent School District (via UT Outreach), https://outreach.uteach.utexas.edu/uteach-outreach-cs-service-learning-program
- Tiny Machine Learning Open Education Initiative, https://tinyml.seas.harvard.edu (Founder)

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PUBLICATIONS

Google Scholar link, https://scholar.google.com/citations?user=gy4UVGcAAAAJ&hl=en&oi=ao

Refereed Conference Proceedings

C1. T. Moseley, A. Shye, **V. Janapa Reddi**, M. Iyer, D. Fay, J. Kihm, A. Settle, D. Grunwald, D. Connors. "Dynamic Run-time Architecture Techniques for Enabling Continuous Optimization," in *ACM International Conference on Computing Frontiers (CF)*, pp.211-220, May 2005. (Acceptance Rate: 43 accepts of 106 submissions, 41%) http://dx.doi.org/10.1145/1062261.1062296

C2. C. Luk, R. Cohn, R. Muth, H. Patil, A. Klauser, G. Lowney, S. Wallace, **V. Janapa Reddi**, K. Hazelwood. "Pin: Building Customized Program Analysis Tools with Dynamic Instrumentation," in *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, vol. 40(6), pp.190-200, June, 2005. (Acceptance Rate: 28 accepts of 135 submissions, 21%) http://dx.doi.org/10.1145/1064978.1065034

C3. S. Figueira, **V. Janapa Reddi**. "Topology-Based Hypercube Structures for Global Communication in Heterogeneous Networks," in *Euro-Par*, pp.994-1004, September 2005. (Acceptance Rate: 121 accepts of 388 submissions, 31%) http://dx.doi.org/10.1007/11549468_109

C4. A. Shye, M. Iyer, **V. Janapa Reddi**, D. Connors. "Code Coverage Testing Using Hardware Performance Monitoring Support," in *IEEE International Symposium on Automated and Analysis-Driven Debugging (AADEBUG)*, pp.159-163, September 2005. (Acceptance Rate: 11 accepts of 30 submissions, 37%) http://dx.doi.org/10.1145/1085130.1085151

C5. Q. Wu, **V. Janapa Reddi**, Y. Wu, J. Lee, D. Connors, M. Martonosi, D. Clark. "A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp.12-282, November 2005. (Acceptance Rate: 29 accepts of 147 submissions, 20%) http://dx.doi.org/10.1109/micro.2005.7

C6. T. Moseley, A. Shye, **V. Janapa Reddi**, D. Grunwald, R. Peri. "Shadow Profiling: Hiding Instrumentation Costs with Parallelism," in *IEEE/ACM International Conference on Code Generation and Optimization (CGO)*, pp.198-208, March 2007. (Acceptance Rate: 27 accepts of 84 submissions, 32%) http://dx.doi.org/10.1109/cgo.2007.35

C7. **V. Janapa Reddi**, D. Connors, R. Cohn, M. Smith. "Persistent Code Caching: Exploiting Code Reuse Across Executions and Applications," in *IEEE/ACM International Conference on Code Generation and Optimization (CGO)*, pp.74-88, March 2007. (Acceptance Rate: 27 accepts of 84 submissions, 32%) http://dx.doi.org/10.1109/cgo.2007.29

C8. A. Shye, T. Mosely, **V. Janapa Reddi**, J. Bloomstedt, D. Connors. "Using Process-Level Redundancy to Exploit Multiple Cores for Transient Fault Tolerance," in *IEEE Dependable Systems and Networks (DSN)*, pp.297-306, June 2007. (Acceptance Rate: 48 accepts of 212 submissions, 23%) http://dx.doi.org/10.1109/dsn.2007.98

C9. **V. Janapa Reddi**, M. Gupta, G. Holloway, G. Wei, M. Smith, D. Brooks. "Voltage Emergency Prediction: Using Signatures to Reduce Operating Margins," *in IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, pp.18-29, February 2009. (Acceptance Rate: 35 accepts of 184, 19%) http://dx.doi.org/10.1109/hpca.2009.4798233

C10. M. Gupta, **V. Janapa Reddi**, G. Holloway, G. Wei, D. Brooks. "An Event-Guided Approach to Reducing Voltage Noise in Processors," in *IEEE Design Automation and Test in Europe*, pp.160-165, April 2009. (Acceptance Rate: 226 of 965 submissions, 23.4%) http://dx.doi.org/10.1109/date.2009.5090651

C11. **V. Janapa Reddi**, M. Gupta, M. Smith, G. Wei, D. Brooks, S. Capmanoni. "Software-Assisted Hardware Reliability: Abstracting Circuit-level Challenges to the Software Stack," in *ACM/EDAC/IEEE Design Automation Conference (DAC)*, pp.788-793, July 2009. (Acceptance Rate: 148 of 684 submissions, 22%) http://dx.doi.org/10.1145/1629911.1630114

C12. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Web Search Using Mobile Cores: Quantifying and Mitigating the Price of Efficiency," in *ACM/IEEE International Symposium on Computer Architecture (ISCA)*, vol. 38(3), pp.314-325, June 2010. (Acceptance Rate: 44 accepts of 245 submissions, 18%) http://dx.doi.org/10.1145/1816038.1816002

C13. **V. Janapa Reddi**, S. Kanev, W. Kim, S. Campanoni, M. Smith, G. Wei, D. Brooks. "Voltage-Guided Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software Thread Scheduling," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp.77-88, December 2010. (Acceptance Rate: 52 accepts of 209 submissions, 25%) http://dx.doi.org/10.1109/micro.2010.35

C14. P. Bailis, **V. Janapa Reddi**, S. Gandhi, D. Brooks, M. Seltzer. "Dimetrodon: Processor-level Preventive Thermal Management via Idle Cycle Injection," in *ACM/EDAC/IEEE Design Automation Conference*, pp.89-94, June 2011. (Acceptance Rate: 156 accepts of 690 submissions, 23%) http://dx.doi.org/10.1145/2024724.2024745

C15. S. Campanoni, T. Jones, G. Holloway, **V. Janapa Reddi**, G. Wei, D. Brooks. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing," in *IEEE/ACM International Symposium on Code Generation and Optimization (CGO)*, pp.84-93, March 2012. (Acceptance Rate: 26 accepts of 90 submissions, 29%) http://dx.doi.org/10.1145/2259016.2259028

C16. **V. Janapa Reddi**, D. Pan, S. Nassif, K. Bowman. "Robust and Resilient Designs from the Bottom Up: Technology, CAD, Circuit, and System Issues," in *IEEE International Symposium on Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp.7-16, Jan. 30 – Feb.2, 2012. (Acceptance Rate: 99 accepts of 288 submissions, 34%) http://dx.doi.org/10.1109/aspdac.2012.6165064

C17. Y. Zhu, **V. Janapa Reddi**. "High-Performance and Energy-Efficient Mobile Web Browsing on Big/Little Systems," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.13-24, February 2013. (Acceptance Rate: 51 accepts of 219 submissions, 23%) http://dx.doi.org/10.1109/hpca.2013.6522303

C18. J. Leng, T. Hetherington, A. ElTantawy, S. Gilani, N. Kim, T. Aamodt, **V. Janapa Reddi**. "GPUWattch: Enabling Energy Optimizations in GPGPUs," in ACM/*IEEE International Symposium on Computer Architecture (ISCA)*, vol. 41(3), pp.487-498, June 2013. (Acceptance Rate: 56 accepts of 288 submissions, 19%) http://dx.doi.org/10.1145/2485922.2485964

C19. Y. Zhu, **V. Janapa Reddi**. "WebCore: Architectural Support for Interactive Mobile Web Browsing," in ACM/*IEEE International Symposium on Computer Architecture (ISCA)*, pp.541-552, June 2014. (Acceptance Rate: 46 accepts of 258 submissions, 18%) http://dx.doi.org/10.1109/isca.2014.6853239

C20. C. Zhou, X. Wang, W. Xu, Y. Zhu, **V. Janapa Reddi,** C. Kim. "Estimation of Instantaneous Frequency Fluctuation in a Fast DVFS Environment Using an Empirical BTI Stress-Relaxation Model," *in IEEE International Symposium on International Reliability Physics Symposium (IRPS)*, pp.2D.2.1-2D.2.6, June 2014. (Acceptance Rate: 114 accepts of 303 submissions, 37%) http://dx.doi.org/10.1109/irps.2014.6860593

C21. J. Leng, Y. Zu, M. Rhu, M. Gupta, **V. Janapa Reddi**. "GPUVolt: Modeling and Characterizing Voltage Noise in GPU Architectures," in IEEE *International Symposium on Low Power Electronics and Design (ISLPED)*, pp.141-146, August 2014. (Acceptance Rate: 63 accepts of 184 submissions, 34%) http://dx.doi.org/10.1145/2627369.2627605

C22. J. Leng, Y. Zu, **V. Janapa Reddi**. "GPU Voltage Noise: Characterization and Hierarchical Smoothing of Spatial and Temporal Voltage Noise Interference in GPU Architectures," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.161-173, February 2015. (Acceptance Rate: 51 accepts of 226 submissions, 23%) http://dx.doi.org/10.1109/hpca.2015.7056030

C23. Y. Zhu, M. Halpern, **V. Janapa Reddi**. "Event-based Scheduling for Energy-Efficient Quality of Service (eQoS) in Mobile Web Applications," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.137-149 February 2015. (Acceptance Rate: 51 accepts of 226 submissions,

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23%)
http://dx.doi.org/10.1109/hpca.2015.7056028

C24. M. Halpern, Y. Zhu, R. Peri, **V. Janapa Reddi**. "Mosaic: Cross-Platform User-Interaction Record and Replay for the Fragmented Android Ecosystem," in *IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)*, pp.215-224, March 2015. (Acceptance Rate: 30 accepts of 92 submissions, 33%) http://dx.doi.org/10.1109/ispass.2015.7095807

C25. J. Leng, A. Buyuktosunoglu, R. Bertran, P. Bose, **V. Janapa Reddi**. "Safe Limits on Voltage Reduction Efficiency in GPUs: A Direct Measurement Approach," in *IEEE International Symposium on Microarchitecture (MICRO)*, pp.294-307, December 2015. (Acceptance Rate: 61 accepts of 283 submissions, 22%) http://dx.doi.org/10.1145/2830772.2830811

C26. Y. Zu, C. R. Lefurgy, J. Leng, M. Halpern, M. S. Floyd, **V. Janapa Reddi**. "Adaptive Guardband Scheduling to Improve System-level Efficiency of the POWER7+," in *IEEE International Symposium on Microarchitecture (MICRO)*, pp.308-321, December 2015. (Acceptance Rate: 61 accepts of 283 submissions, 22%) http://dx.doi.org/10.1145/2830772.2830824

C27. Y. Zhu, D. Richins, M. Halpern, **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Server-side Web Applications," in IEEE *International Symposium on Microarchitecture (MICRO)*, pp.762-774, December 2015. (Acceptance Rate: 61 of 283 submissions, 22%) http://dx.doi.org/10.1145/2830772.2830792

C28. M. Halpern, Y. Zhu, **V. Janapa Reddi**. "Mobile CPU's Rise to Power: Quantifying the Impact of Generational Mobile CPU Design Trends on Performance, Energy, and User Satisfaction," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, pp.64-76, March 2016. (Acceptance Rate: 53 accepts of 240 submissions, 22%) http://dx.doi.org/10.1109/hpca.2016.7446054

C29. Y. Zhu, **V. Janapa Reddi**. "GreenWeb: Language Extensions for Energy Efficient Mobile Web Computing," in *ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, pp.145-160, June 2016. (Acceptance Rate: 49 accepts of 304 submissions, 16%) http://dx.doi.org/10.1145/2908080.2908082

C30. Y. Liu, Z. Yu, L. Eeckhout, **V. Janapa Reddi**, Y. Luo, X. Wang, Z. Wang, C. Xu. "Barrier-Aware Warp Scheduling for Throughput Processors," in *ACM International Conference on Supercomputing (ICS)*, June 2016. (Acceptance Rate: 43 accepts of 178 submissions, 24%) http://dx.doi.org/10.1145/2925426.2926267

C31. N. Chachmon, D. Richins, R. Cohn, M. Christensson, W. Cui, **V. Janapa Reddi**. "Simulation and Analysis Engine for Scale-out Workloads," in *ACM International Conference on Supercomputing (ICS)*, June 2016. (Acceptance Rate: 43 accepts of 178 submissions, 24%) http://dx.doi.org/10.1145/2925426.2926293

C32. Y. Zu, W. Huang, I. Paul, **V. Janapa Reddi**. "Ti states: Processor Power Management in the Temperature Inversion Region," in IEEE *International Symposium on Microarchitecture (MICRO)*, October 2016. (Acceptance Rate: 21 accepts of 283 submissions, 22%) http://dx.doi.org/10.1109/MICRO.2016.7783758

C33. M. Kazdagli, **V. Janapa Reddi**, M. Tiwari. "Quantifying and Improving the Efficiency of Hardware-based Mobile Malware Detectors," in IEEE *International Symposium on Microarchitecture (MICRO)*, October 2016. (Acceptance Rate: 21 accepts of 283 submissions, 22%) http://dx.doi.org/10.1109/MICRO.2016.7783740

C34. A. Zou, J. Leng, Y. Zu, T. Tong, **V. Janapa Reddi**, D. Brooks, G. Y. Wei, X. Zhang. "Ivory: Early-Stage Design Space Exploration Tool for Integrated Voltage Regulators," in Proceedings of the 54th *Annual Design Automation Conference (DAC)*, June 2017. (Acceptance Rate: 152 accepts of 674 submissions, 22.6%) http://dx.doi.org/10.1145/3061639.3062268

C35. D. Richins, T. Ahmed, R. Clapp, **V. Janapa Reddi**, "Amdahl's Law in Big Data Analytics: Alive and Kicking in TPCx-BB (BigBench)," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, March 2018.

C36. A. Zou, J. Leng, X. He, Y. Zu, **V. Janapa Reddi**, X. Zhang. "Efficient and Reliable Power Delivery in Voltage-Stacked Manycore System with Hybrid Charge-Recycling Regulators," in Proceedings of the 55th *Annual Design Automation Conference (DAC)*, June 2018. (Acceptance Rate: 168 papers accepted out of 691 submitted, 24.3%)

C37. B. Boroujerdian, H. Genc, S. Krishnan, W. Cui, A. Faust, **V. Janapa Reddi**. "MAVBench: Micro Aerial Vehicle Benchmarking," in *IEEE International Symposium on Microarchitecture (MICRO)*, pp.894-907, October 2018. (Acceptance Rate: 74 papers accepted out of 348 submitted, 21.2%) http://dx.doi.org/10.1109/MICRO.2018.00077

C38. A. Zou, J. Leng, X. He, Y. Zu, C. D. Gill, **V. Janapa Reddi**, Xuan Zhang. "Voltage-Stacked GPUs: A Control Theory Driven Cross-Layer Solution for Practical Voltage Stacking in GPUs," in *IEEE/ACM International Symposium on Microarchitecture (MICRO)*, pp. 390-402, October 2018, https://doi.org/10.1109/MICRO.2018.00039 (Acceptance Rate: 74 papers accepted out of 348 submitted, 21.2%)

C39. M. Hill, **V. Janapa Reddi**. "Gables: A Roofline Model for Mobile SoCs," in IEEE *International Symposium on High Performance Computer Architecture (HPCA)*, February 2019 https://doi.org/10.1109/HPCA.2019.00047 (Acceptance Rate: 9 papers accepted out of 18 submitted – industry session, 50%)

C40. Y. Zu, D. Richins, C. Lefurgy, **V. Janapa Reddi**. "Fine-Tuning the Active Timing Margin (ATM) Control Loop for Maximizing Multi-Core Efficiency on an IBM POWER Server," in IEEE *Proceedings of the 25th International Symposium on High Performance Computer Architecture (HPCA)*, 2019. https://doi.org/10.1109/HPCA.2019.00031 (Acceptance Rate: 9 papers accepted out of 18 submitted, 50%)

C41. W. Cui, D. Richins, Y. Zhu, **V. Janapa Reddi**. "Tail Latency in Node.js: Energy Efficient Turbo Boosting for Long Latency Requests In Event-Driven Web Services," in *ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (VEE)*, 2019. https://doi.org/10.1145/3313808.3313823 (Acceptance Rate: 15 papers accepted out of 33 submitted, 45.5%)

C42. M. Halpern, B. Boroujerdian, T. Mummert, E. Duesterwald, **V. Janapa Reddi**, "One Size Does Not Fit All: Quantifying and Exposing the Accuracy-Latency Trade-off in Machine Learning Cloud Service APIs via Tolerance Tiers," in *IEEE Proceedings of the 19th International Symposium on Performance Analysis of Systems and Software (ISPASS)*, 2019. https://doi.org/10.1109/ISPASS.2019.00012 (Acceptance Rate: 26 papers accepted out of 88 submitted, 29.5%)

C43. D. Richins, D. Doshi, M. Blackmore, A. T. Nair, N. Pathapati, A. Patel, B. Daguman, D. Dobrijalowski, R. Illikkal, K. Long, D. Zimmerman, **V. Janapa Reddi**, "Missing the Forest for the Trees: End-to-End AI Application Performance in Edge Data Centers" in *IEEE Proceedings of the 26th International Symposium on High Performance Computer Architecture (HPCA)*, 2020. (Acceptance Rate: 6 papers accepted out of 15 submitted, 40%)

C44. Jingwen Leng, Alper Buyuktosunoglu, Ramon Bertran, Pradip Bose, Quan Chen, Minyi Guo, **V. Janapa Reddi**, "Asymmetric resilience: Exploiting task-level idempotency for transient error recovery in accelerator-based systems" *in IEEE International Symposium on High Performance Computer Architecture (HPCA)*, 2020. https://doi.org/10.1109/hpca47549.2020.00014

C45. T. Tambe, E. Yang, Z. Wan, Y. Deng, **V. Janapa Reddi**, Alexander Rush, David Brooks, Gu-Yeon Wei, "Algorithm-Hardware Co-Design of Adaptive Floating-Point Encodings for Resilient Deep Learning Inference" in *57th ACM/IEEE Design Automation Conference (DAC)*, 2020. https://doi.org/10.1109/dac18072.2020.9218516

C46. J. Gleeson, S. Krishnan, M. Gabel, **V. Janapa Reddi**, Eyal de Lara, Gennady Pekhimenko, "RL-Scope: Cross-Stack Profiling for Deep Reinforcement Learning Workloads" in *Proceedings of Machine Learning Systems (MLSys)*, 2021.

C47. C. Banbury, C. Zhou, I. Fedorov, R. Navarro, U. Thakkar, D. Gope, **V. Janapa Reddi**, Matthew Mattina, Paul N Whatmough, "MicroNets: Neural Network Architectures for Deploying TinyML Applications on Commodity Microcontrollers" in *Proceedings of Machine Learning Systems (MLSys)*, 2021.

C48. M. Buch, Z. Azad, A. Joshi, and **V. Janapa Reddi**, "AI Tax in Mobile SoCs: End-to-end Performance Analysis of Machine Learning in Smartphones," in *2021 IEEE International Symposium on Performance Analysis of Systems and Software, ISPASS '21*, Virtual, Stony Brook, NY, March 28-30, 2021.

C49. M. Lam, S. Chitlangia, S. Krishnan, Z. Wan, G. Barth-Maron, A. Faust, **V. Janapa Reddi**, "ActorQ: Quantization for Actor-Learner Distributed Reinforcement Learning," in *ICLR, Hardware Aware Efficient Training Workshop at ICLR 2021*, Virtual, May 7, 2021.

C50. D. Richins, D. Doshi, M. Blackmore, A. Thulaseedharan Nair, N. Pathapati, A. Patel, B. Daguman, D. Dobrijalowski, R. Illikkal, K. Long, D. Zimmerman, **V. Janapa Reddi**, "AI Tax: The Hidden Cost of AI Data Center Applications," in *ACM Transactions on Computer Systems (TOCS)*, vol. 37, no. 1-4, pp. 1-32, 2021.

C51. M. Mazumder, C. Banbury, J. Meyer, P. Warden, and **V. Janapa Reddi**, "Few-Shot Keyword Spotting in Any Language," in *INTERSPEECH 2021*, Virtual, Brno, Czech Republic, 2021.

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Technical Reports

TR1. **V. Janapa Reddi**, B. Lee, T. Chilimbi, K. Vaid. "Web Search Using Small Cores: Quantifying the Price of Efficiency," in Microsoft Research Tech. Report, June 2010.

Theses

Th1. **V. Janapa Reddi**. "Heterogeneous Networks of Workstations Across Wide Area Networks," B.S. Thesis, Department of Electrical and Computer Engineering, Santa Clara University. June 2003.

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Th2. **V. Janapa Reddi**. "Deploying Dynamic Code Transformation in Modern Computing Environments," M.S. Thesis, Department of Electrical and Computer Engineering, University of Colorado. November 2005.
Th3. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability: Enabling Aggressive Timing Speculation Using Run-Time Feedback from Hardware and Software," Ph.D. Thesis, School of Engineering and Applied Sciences, Harvard University. March 2010.

ORAL PRESENTATIONS

Invited Talks and Seminars
T1. **V. Janapa Reddi**. "Persistent Code Caching," Intel, Santa Clara–CA, March 2007.
T2. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Intel, Santa Clara–CA, March 2010.
T3. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," AMD, Austin–TX, March 2010.
T4. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Microsoft Research, Redmond–WA, June 2010.
T5. **V. Janapa Reddi**. "Web Search Using Small Cores," Amazon, Seattle–WA, June 2010.
T6. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," Intel, Portland–OR, July 2010.
T7. **V. Janapa Reddi**. "Software-Assisted Hardware Reliability," IBM T. J. Watson Labs, Yorktown–NY, July 2010.
T8. **V. Janapa Reddi**. "Web Search Using Small Cores," SeaMicro, Santa Clara–CA, July 2010.
T9. **V. Janapa Reddi**. "Web Search Using Small Cores," Google, Palo Alto–CA, July 2010.
T10. **V. Janapa Reddi**. "Web Search Using Small Cores," HP Labs, Palo Alto–CA, July 2010.
T11. **V. Janapa Reddi**. "Web Search Using Small Cores," Facebook, Palo Alto–CA, July 2010.
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T13. **V. Janapa Reddi**. "Web Search Using Small Cores," Intel, Hudson–MA, July 2010.
T14. **V. Janapa Reddi**. "Web Search Using Small Cores," AMD, Boxborough–MA, October 2010.
T15. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," Intel, Austin–TX, August 2012.
T16. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," *AMD*, Austin–TX, August 2012.
T17. **V. Janapa Reddi**. "Toward High-Performance and Energy-Efficient Mobile Web Browsing," Qualcomm, Santa Clara–MA, February 2013.
T18. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," Intel, Austin–TX, February 2014.
T19. **V. Janapa Reddi**. "Robust and Resilient Systems from the Bottom-Up: Circuits, Architecture and Software Integration," ISSCC Forum, San Francisco–CA, February 2014.
T20. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," Samsung, Austin–TX, March 2014.
T21. **V. Janapa Reddi**. "Architectural Support for the Interactive Mobile Web," *ARM*, Austin–TX, March 2014.
T22. **V. Janapa Reddi**. "Mobile Processor Architectures: Design Implications and Challenges for Energy Efficiency," Indo-American Frontiers of Engineering (IAFOE), Mysore–India, May 2014.
T23. **V. Janapa Reddi**. "Hardware and Software Co-Design for Robust and Resilient Execution," International Conference on Integrated Circuit Design and Technology (ICICDT), Austin–TX, May 2014.
T24. **V. Janapa Reddi**. "Architecting for the Mobile Web: Where We've Been, Where We're Heading, and What We Need to Address," Parallelism in Mobile Platforms (PRISM) held in conjunction with International Symposium on Computer Architecture, June 2014.
T25. **V. Janapa Reddi**. "Simulators are Perfect, Authors are Oracles, Users are Innocent," Workshop on Duplicating, Deconstructing and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture, June 2014.

T26. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Univ. of Michigan, November 2014.
T27. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Intel, Santa Clara–CA, February 2015.
T28. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Facebook, Menlo Park–CA, March 2015.
T29. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Microsoft, Seattle–WA, April 2015.
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T31. **V. Janapa Reddi**. "Voltage Noise in Multicore Processors," Intel, Portland–OR, May 2015.
T32. **V. Janapa Reddi**, "GPU Voltage Guardband Management to Achieve Exascale Energy-Efficiency," Intel, Portland–OR, May 2015.
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T35. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Taiwan Application Processor Union – Mobile SoC Summer Course, Taiwan, September 2015.
T36. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," Mediatek, Taiwan, September 2015.
T37. **V. Janapa Reddi**. "What Users Want and What Hardware Provides: Bridging the Gap Between User Quality of Experience (QoE) and Mobile Device Trends," National Taiwan University, Taiwan, September 2015.
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T40. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Google Faculty Summit, October 2015.
T41. **V. Janapa Reddi**. "Watt-Wise Web: Architecting for a Responsive and Energy-Efficient Mobile Web," Texas A&M University, November 2015.
T42. **V. Janapa Reddi**. "Programming the Web of Things," Workshop on Internet of Things (IoT) held in conjunction with International Symposium on Microarchitecture, Hawaii, December 2015.
T43. **V. Janapa Reddi**. "End of the Road for My CAREER," Workshop on Negative Outcomes, Post-mortems, and Experiences (NOPE) held in conjunction with International Symposium on Microarchitecture, Hawaii, December 2015.
T44. **V. Janapa Reddi**. "From Moore's Law to Moore's Crawl: Architecting the Next-Generation of Mobile Computing Devices," University of Washington, Seattle–WA, February 2016.
T45. **V. Janapa Reddi**. "From Moore's Law to Moore's Crawl: Architecting the Next-Generation of Mobile Computing Devices," National Academy of Engineering (NAE) Annual Event, Irvine–CA, February 2016.
T46. **V. Janapa Reddi**. "Programming the Web of Things: Why Architects Should Care," Sensors to Cloud Architectures Workshop, Barcelona, March 2016. **(Keynote)**
T47. **V. Janapa Reddi**. "Mobile CPU Evolution: The Past, the Present, and the Future," Rice University – TexasWISE Keynote, Houston, May 2016.
T48. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," Intel, Santa Clara–CA, May 2016.
T49. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," AMD, Austin–TX, May 2016.

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T50. **V. Janapa Reddi**. "Microarchitectural Implications of Event-driven Programming," Northwestern, Chicago–IL, May 2016.
T51. **V. Janapa Reddi**. "Watt-Wise-Web://Architecting for Responsiveness and Energy-Efficiency," The University of Chicago, Chicago–IL, May 2016.
T52. **V. Janapa Reddi**. "Architecture Support for Scripting from Mobile to Cloud," Stanford University, Palo Alto, February 2017.
T53. **V. Janapa Reddi**. "Architecting for Big Data Analytics: Think Dubai rather than Venice," Workshop on BigData Benchmarks, Performance, Optimization and Emerging Hardware (co-located with ASPLOS), March 2018.
T54. **V. Janapa Reddi**. "Aerial Computing: Challenges and Opportunities for Hardware and Software Architects Designing Flying Systems," IBM T. J. Watson, April 2018.
T55. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators, and ML cloud and edge platforms," Samsung Austin Research Center (SARC), October 2018.
T56. **V. Janapa Reddi**. "Mobile Robotics for Computer Architects," First Annual Workshop on Domain Specific System Architecture co-located with International Symposium on Microarchitecture (MICRO), October 2018. **(Keynote)**
T57. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators, and ML cloud and edge platforms," Samsung Advanced Computing Lab (ACL), November 2018.
T58. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators, and ML cloud and edge platforms," IEEE BigBench co-located with the IEEE Big Data Conference, December 2018. **(Keynote)**
T59. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators in Cloud and Edge Computing," The Forum of Turing Centers, Shanghai Jiao Tong University, December 2018. **(Keynote)**
T60. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators in Cloud and Edge Computing," Boston Area Computer Architecture Workshop, December 2018. **(Keynote)**
T61. **V. Janapa Reddi**. "Autonomous Aerial Computing Machines," International Workshop on Performance Analysis of Machine Learning Systems, March 2019.
T62. **V. Janapa Reddi**. "Evaluating Resiliency in End-to-end Learning for Autonomous Machines," The 15th Workshop on Silicon Errors in Logic – System Effects, March 2019.
T63. **V. Janapa Reddi**. "The Vision Behind MLPerf (mlperf.org)," Intel VSSAD, March 2019.
T64. **V. Janapa Reddi**. "Ten Commandments for Mobile Computer Architecture," Workshop on Infrastructure and Methodology for SoC-level Performance and Power Modeling, co-located with ASPLOS, April 2019.
T65. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators in Cloud and Edge Computing," Synopsis SNUG, Taiwan, September 2019.
T66. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators in Cloud and Edge Computing," Taiwan AI Labs, September 2019. **(Keynote)**
T67. **V. Janapa Reddi**. "The Vision Behind MLPerf: A broad ML benchmark suite for measuring the performance of ML software frameworks, ML hardware accelerators in Cloud and Edge Computing," Taiwan Semiconductor Manufacturing Company (TSMC), September 2019.
T68. **V. Janapa Reddi**. "The Vision Behind MLPerf" Advanced Micro Devices (AMD) Tech Talk, June 2020.
T69. **V. Janapa Reddi**. "The Vision Behind MLPerf" International Solid-State Circuits Conference (ISSCC), February 2020.
T70. **V. Janapa Reddi.** "MLPerf Inference" Machine Learning Systems (MLSys) Workshop, February 2020.

T71. **V. Janapa Reddi.** "tinyMLPerf: Benchmarking Ultra-low-power Systems" Tiny Machine Learning Summit, March 2020.
T72. **V. Janapa Reddi.** "tinyMLPerf: Benchmarking Ultra-low-power Systems", "Machine Learning at the Edge" Workshop co-located with Design Automation Conference, March 2021.
T73. **V. Janapa Reddi.** "tinyMLPerf: Benchmarking Ultra-low-power Systems" Tiny Machine Learning Summit, March 2021.
T74. **V. Janapa Reddi**. "The Vision Behind MLPerf" STMicroelectronics, July 2021.
T75. **V. Janapa Reddi**. "Tiny Machine Learning" Workshop on Artificial Intelligence, Machine Learning, & Computational Intelligence, July 2021.
T76. **V. Janapa Reddi**. "The Vision Behind MLPerf" Tensorrent, September 2021.
T77. **V. Janapa Reddi**. "The Vision Behind MLPerf" SiFive Engineering Forum, October 2021.
T78. **V. Janapa Reddi**. "The Vision Behind MLPerf" Samsung AI Cambridge, October 2021.
T79. **V. Janapa Reddi.** "Widening Access to Applied Machine Learning with TinyML" IEEE Global Humanitarian Technology Conference, October 2021. **(Keynote)**
T80. **V. Janapa Reddi.** "Democratizing TinyML" MICRO 2021 Workshop on Systems for Multi-DNN Workloads, October 2021. **(Keynote)**
T81. **V. Janapa Reddi.** "Democratizing TinyML: Generalization, Standardization and Automation" Workshop on Hardware and Algorithms for Learning On-a-chip (HALO) workshop at the ICCAD conference, November 2021. **(Keynote)**
T82. **V. Janapa Reddi.** "Democratizing TinyML: Generalization, Standardization and Automation" Multi-DNN Workshop, co-located with MICRO, November 2021. **(Keynote)**
T83. **V. Janapa Reddi.** "Tiny Machine Learning (TinyML) for Robotics" Conference on Robot Learning, November 2021. **(Keynote)**
T84. **V. Janapa Reddi.** "Data for TinyML" Data for AI Summit @Google (internal), November 2021. **(Keynote)**
T85. **V. Janapa Reddi.** "Tiny Machine Learning" EdukCircle International Convention on Engineering and Computer Technology, November 2021.
T86. **V. Janapa Reddi.** "Machine Learning's Future is Tiny & Bright" AICON GWANGJU, December 2021. **(Keynote)**
T87. **V. Janapa Reddi.** "Democratizing TinyML" Globecom Workshop on Sustainable Environmental Sensing Systems, December 2021. **(Keynote)**
T88. **V. Janapa Reddi.** "Tiny Machine Learning" Accelerated Machine Learning Workshop, co-located with HiPEAC 2022, January 2022.
T89. **V. Janapa Reddi.** "IoT 2.0: The Era of Intelligence on Things" Design Automation and Test in Europe, March 2022.
T90. **V. Janapa Reddi.** "Tiny Machine Learning (TinyML) for Domain-Specific Systems" International Workshop on Domain Specific System Architecture (DOSSA-4), April 2022.
T91. **V. Janapa Reddi.** "Democratizing TinyML" Rutgers Efficient AI (REFAI) Seminar, May 2022.
T92. **V. Janapa Reddi.** "Machine Learning Metrics" HiPEAC AccML Workshop, June 2022.
T93. **V. Janapa Reddi.** "Tiny Machine Learning: Challenges and Opportunities" Design Automation Conference, ROAD4NN Workshop, July 2022. **(Keynote)**
T94. **V. Janapa Reddi.** "Tiny Machine Learning: A System-level Perspective" ACM/IEEE International Symposium on Low Power Electronics and Design, August 2022. **(Keynote)**
T95. **V. Janapa Reddi.** "The Future of Smart Cities is Tiny and Bright" ACM International Conference on Future Energy Systems (ACM e-Energy), July 2022. **(Keynote)**
T96. **V. Janapa Reddi.** "The Vision Behind MLPerf and DataPerf" Monterey Data Conference, August 2022.
T97. **V. Janapa Reddi.** "DataPerf: Benchmarks for Data-centric AI Development" The Future of Data-Centric AI, Snorkel.ai, August 2022.

T98. **V. Janapa Reddi.** “Tiny Machine Learning" Chips & Compilers Symposium at MLSys ‘22, September 2022.
T99. **V.Janapa Reddi.** “Benchmarking FastML Systems” Fast ML for Science Workshop, September 2022.
T100. **V.Janapa Reddi.** “MLPerf & DataPerf” The Autonomous Vehicle Computing Consortium (AVCC), September 2022.
T101. **V.Janapa Reddi.** “ML Metrics: The Past, Present, and Future of Benchmarking ML Systems, Datasets, and Use Cases” Specialization with Benchmarks for Emerging Applications (MICRO), October 2022
T102. **V.Janapa Reddi.** Urban Sensor Networks Workshop Panel, November 2022
T103. **V.Janapa Reddi.** IEEE International Symposium on Low-Power and High-Speed Chips (COOL Chips), April 2023
T104. **V.Janapa Reddi.** Keynote at MICRON, April 2023
T105. **V.Janapa Reddi.** "The Parameter and Chip Wars: Shifting the Focus from Model-centric to Data-centric AI", April 2023
T106. **V.Janapa Reddi.** NeuroBench: Advancing Neuromorphic Computing through Collaborative and Rigorous Benchmarking, April 2023
T107. **V.Janapa Reddi.** Future of datacentric AI talk, July 2023
T108. **V.Janapa Reddi.** FDCAI "Adopting AI: With Power Comes Responsibility" Panel, June 2023
T109. **V.Janapa Reddi.** “The Parameter and Chip Wars”, Vail Computer Elements Workshop, June 2023
T110. **V.Janapa Reddi.** "Architecture 2.0"Design Automation Conference (DAC), July 2023

Other Major Presentations

M1. R. Cohn and **V. Janapa Reddi**. “Software Instrumentation and Hardware Profiling for Intel Itanium Linux,” International Symposium on Code Generation and Optimization (CGO), 2004.
M2. C. Luk, D. Connors, W. Hsu, T. Moseley, **V. Janapa Reddi**. “Software Instrumentation as a Tool for Architecture and Compiler Research,” International Symposium on Architectural Support for Programming Languages and Operating (ASPLOS), 2004.
M3. K. Hazelwood and **V. Janapa Reddi**. “Using Pin for Compiler and Computer Architecture Research and Education,” International Symposium on Programming Language Design and Implementation (PLDI), 2007.
M4. K. Hazelwood, **V. Janapa Reddi**, D. Kaeli, D. Connors. “Hands-on Pin! for Architecture, OS and Program Analysis Research,” International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2007.
M5. S. Campanoni and **V. Janapa Reddi**. “ILDJIT Compiler Framework for Architecture Research,” International Symposium on Microarchitecture (MICRO), 2010.
M6. **V. Janapa Reddi.** “Hardware and Software Co-design for Robust and Resilient Execution,” International Conference on IC Design and Technology (ICICDT), 2012.
M7. N. Chachmon, M. Christensson, R. Cohn, **V. Janapa Reddi.** “SIMICS 2015: System-level Program Analysis and Architectural Evaluation with Simics,” International Symposium on Performance Analysis of Systems and Software (ISPASS), 2015.
M8. N. Chachmon, M. Christensson, R. Cohn, **V. Janapa Reddi.** “SIMICS 2015: System-level Program Analysis and Architectural Evaluation with Simics,” International Symposium on Workload Characterization (IISWC), 2015.
M9. N. Chachmon, M. Christensson, **V. Janapa Reddi.** “Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis,” International Symposium on High Performance Computer Architecture (HPCA,), 2016.
M10. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** “Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis,” International Symposium on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2016.

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M11. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Conference on Supercomputing (ICS), 2016.
M12. N. Chachmon, D. Richins, M. Christensson, **V. Janapa Reddi.** "Intel SAE: A Dynamic Binary Instrumentation Framework for Full-System Simulation and Analysis," International Symposium on Computer Architecture (ISCA), 2016.
M13. Y. Zhu, M. Halpern, **V. Janapa Reddi.** "MobiTools: Tutorial on Infrastructure and Tools for Mobile Computer Architecture Research with an Emphasis on Real System Measurement," International Symposium on Computer Architecture (ISCA), 2016.
M14. D. Richins, B. Gowda, N. Chachmon, M. Christensson, **V. Janapa Reddi.** "BigBench+SAE: Instrumenting an Industry-strength BigData Benchmark for BigData Analytics," International Symposium on Microarchitecture (MICRO), 2016.
M15. S. Prakash, **V. Janapa Reddi.** "CFU Playground," IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2022.

PATENTS

P1. R. Cohn, T. Moseley, and **V. Janapa Reddi**. "System and method to instrument references to shared memory." U.S. Patent Application 11/143,130, filed June 1, 2005.
P2. N. Kim, J. O'Connor, M. Schulte, and **V. Janapa Reddi**. "Method and apparatus for power reduction during lane divergence." U.S. Patent Application 13/605,460, filed September 6, 2012.
P3. **V. Janapa Reddi**, M. Gupta, G. Holloway, G. Wei, M. D. Smith, and D. Brooks. "Adaptive event-guided system and method for avoiding voltage emergencies." U.S. Patent 8,949,666, issued February 3, 2015.

PH.D. STUDENTS

A. Current students:
   a. Behzad Boroujerdian
   b.
   c. Colby Banbury
   d. Daniel Richins
   e. Mark Mazumder
   f. Max Lam
   g. Radhika Ghosal
   h. Shvetank Prakash
   i. Srivatsan Krishnan
   j. Yu-shun Hsian

B. Graduated students:
   a. Sabrina Neuman (Jun 2023), Assistant Prof. at Boston University
   b. Brian Plancher (Dec 2020), Assistant Prof. at Barnard College at University of Columbia
   c. Yazhou Zu (Dec 2018), Google
   d. Yuhao Zhu (Jun 2016), Assistant Prof. at Univ. of Rochester (CS)
   e. Jingwen Leng (Dec 2016), Assistant Prof. at Shanghai Jiao Tong University (CSE)

M.S. STUDENTS

A. Students graduated:
   a. Jonathan Cruz (May 2021)
   b. Wenzhi Cui (December 2017)

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c. Matthew Halpern (June 2017)
d. Aditya Srikanth (May 2013)
e. Ankita Garg (co-supervised, May 2013)

BIO

Vijay Janapa Reddi is an Associate Professor at Harvard University, Vice President, and Founding Member of MLCommons (mlcommons.org), a nonprofit organization devoted to accelerating machine learning (ML) innovation for all. He co-chairs the MLCommons Research organization and sits on the board of directors of MLCommons. He co-led the development of the MLPerf Inference benchmark for IoT, mobile, edge, and datacenter applications. Before moving to Harvard, he was an Associate Professor at The University of Texas at Austin's Department of Electrical and Computer Engineering. He specializes in developing mobile and edge computing platforms, as well as the Internet of Things. His work is largely based on runtime systems, computer architecture, and applied machine learning methods. Numerous accolades and awards have been awarded to Dr. Janapa-Reddi, including the Gilbreth Lecturer Honor from the National Academy of Engineering (NAE) in 2016, the IEEE TCCA Young Computer Architect Award (2016), the Intel Early Career Award (2013), the Google Faculty Research Awards in 2012, 2013, 2015, 2017, and 2020, the Best Papers at the 2020 Design Automation Conference (DAC), the 2005 International Symposium on Microarchitecture (MICRO), and the 2009 International Symposium on High-Performance Computer Architecture (HPCA). Additionally, he has won various honors and awards, including IEEE Top Picks in Computer Architecture (2006, 2010, 2011, 2016, 2017, 2022, 2023). The MICRO and HPCA Halls of Fame include him (inducted in 2018 and 2019, respectively). He is strongly devoted to expanding access to applied machine learning for STEM, diversity, and the application of AI for social good. To merge embedded systems and machine learning, he developed the Tiny Machine Learning (TinyML) series on edX, a massive open online course (MOOC) that thousands of students worldwide can access and audit for free. Additionally, he oversaw the Austin Hands-on Computer Science (HaCS) program, which the Austin Independent School District used to teach CS to students in grades K-12. Dr. Janapa-Reddi holds degrees in computer science from Harvard University, electrical and computer engineering from the University of Colorado at Boulder, and computer engineering from Santa Clara University. Dr. Janapa-Reddi's life's passion is dedicated to helping individuals and teams succeed while making the world a better place, one bit at a time.