Bottom-up Filling of Surfactant-catalyzed CVD of Copper and Copper-manganese Alloy in Narrow Trenches

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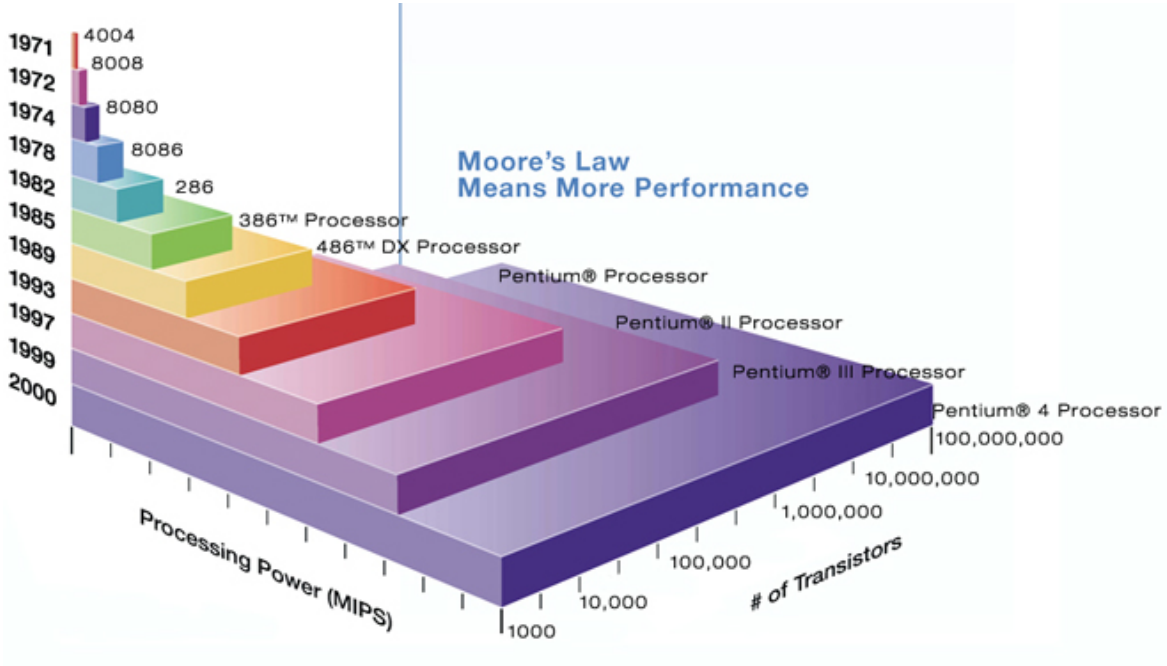
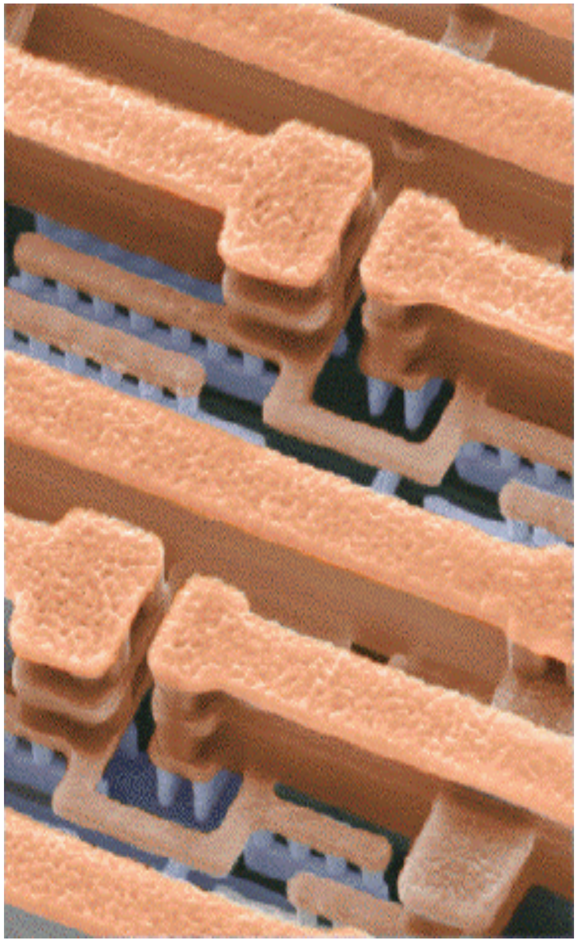
Introduction

- Periodic improvements in performance of microelectronic devices have been achieved through device-scaling

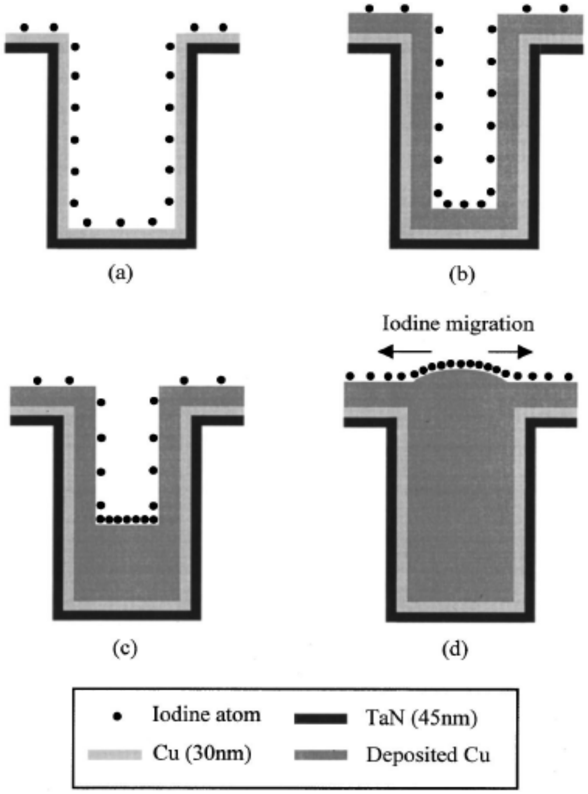


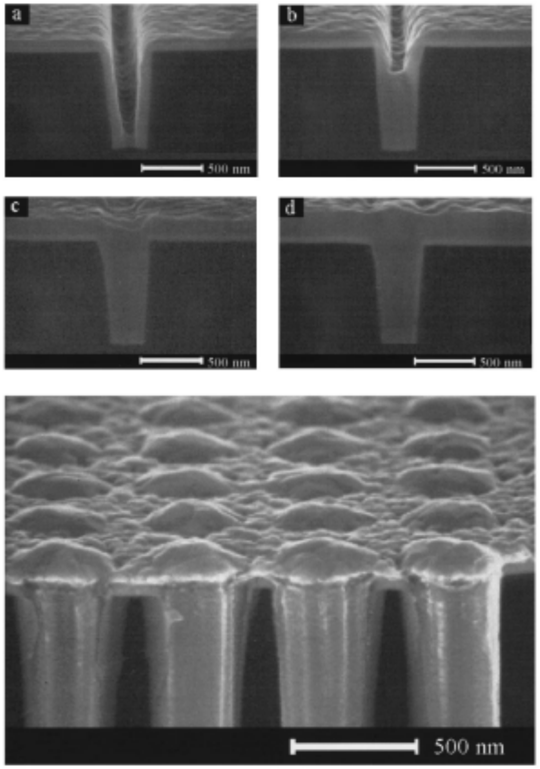


- Damascene process (EP and CMP) is commonly adopted for patterning copper
- Conventional techniques lead to formation of voids and seams in nanoscale trenches and via holes

Surfactant Catalyzed Bottom-up Filling of Copper

- Iodine is a catalytic surfactant that promotes better morphology and higher deposit rate
- Bottom-up filling of sub-micrometer features could be achieved



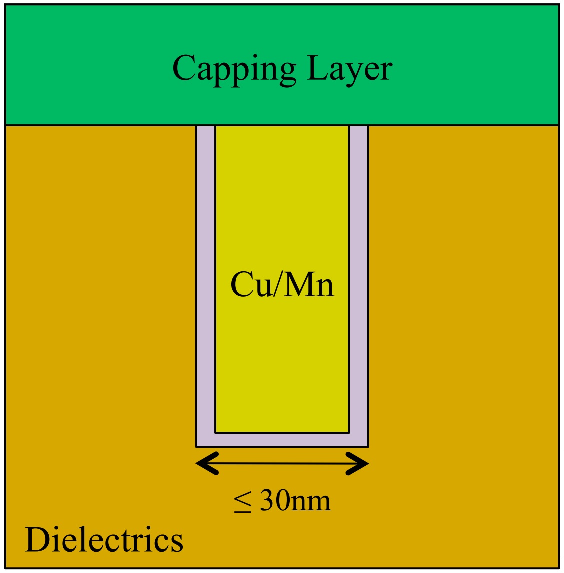


- This process requires a conformal Cu seed layer on top of the diffusion barrier and adhesion layer

E.S. Hwang and J. Lee, “Surfactant-Catalyzed Chemical Vapor Deposition of Copper Thin Films”, *Chem. Mater.*,**12**, 2076 (2000).
K. Shim, O. Kwon, H. Park, W. Koh, and S. Kang, “Bottom-up Filling of Submicrometer Features in Catalyst-Enhanced Chemical Vapor Deposition of Copper”, *J. Electrochem. Soc.*, **149** (2) G109-G113 (2002) .

Surfactant Catalyzed CVD Cu and CuMn in Narrow Trenches

Motivation



Key Points

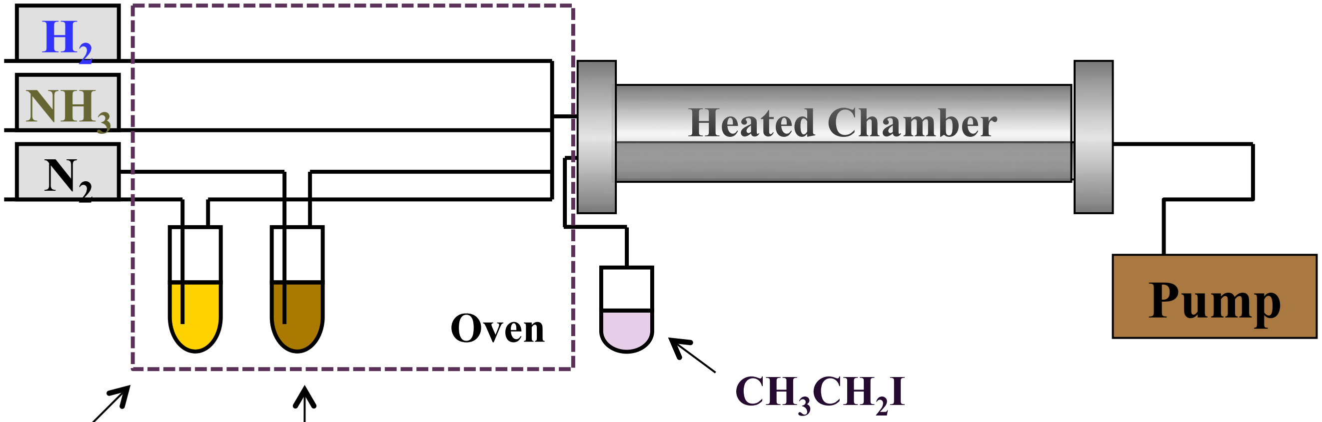
- Conformally deposited manganese nitride serves as a barrier/adhesion layer
- Iodine acts as a surfactant catalyst to promote Cu and Mn growth
- Void-free, bottom-up filling of Cu or Cu-Mn alloy in narrow trenches with aspect ratio ≥ 5:1
- Mn diffuses out from Cu during post-annealing to further improves adhesion and barrier properties at Cu/insulator interface

Y. Au, Y. Lin and R.G. Gordon, “Filling Narrow Trenches by Iodine-Catalyzed CVD of Copper and Manganese on Manganese Nitride Barrier/Adhesion Layers”, *J. Electrochem. Soc.*, **158** (5) D248-D253 (2011).

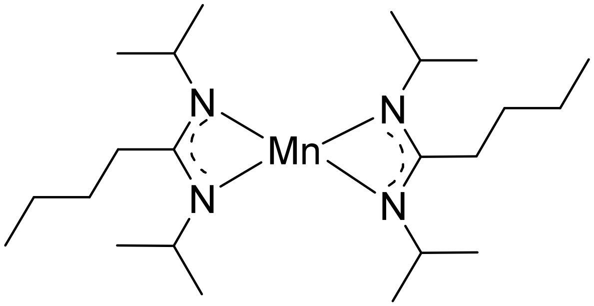
Chemical Vapor Deposition of Copper

CVD System

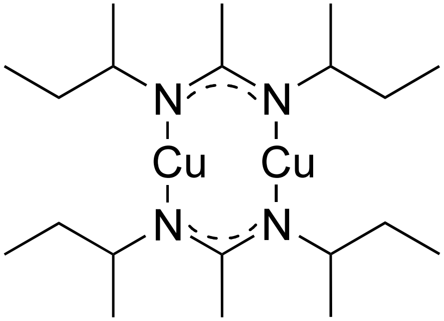
Temperature
130°C for Mn_4N
180°C for Cu and CuMn
Pressure: 5 Torr



Precursors



Bis ***(N,N'-diisopropylpentylamidinato) manganese(II)***
Melting Point: ~60°C
Bubbler Temperature: 90°C
Vapor Pressure: ~0.1 mbar at 90°C



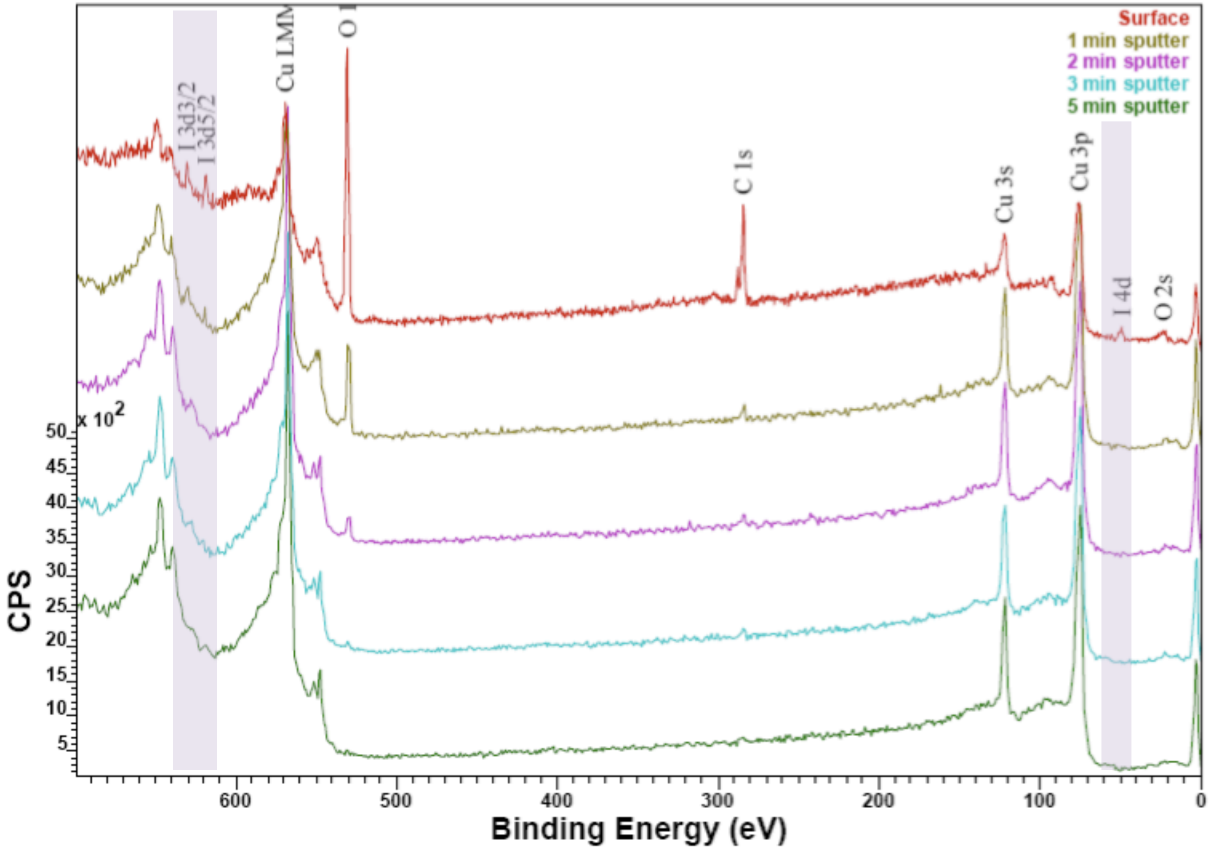
Copper (I) N,N'-di-sec-butylacetamidinate
Melting Point: ~75°C
Bubbler Temperature: 130°C
Vapor Pressure: ~0.25 mbar at 95°C

Advantages of metal amidinate precursors:

- Chelating effect enhances thermal stability
- Low carbon and oxygen contamination
- Tunable reactivity and volatility

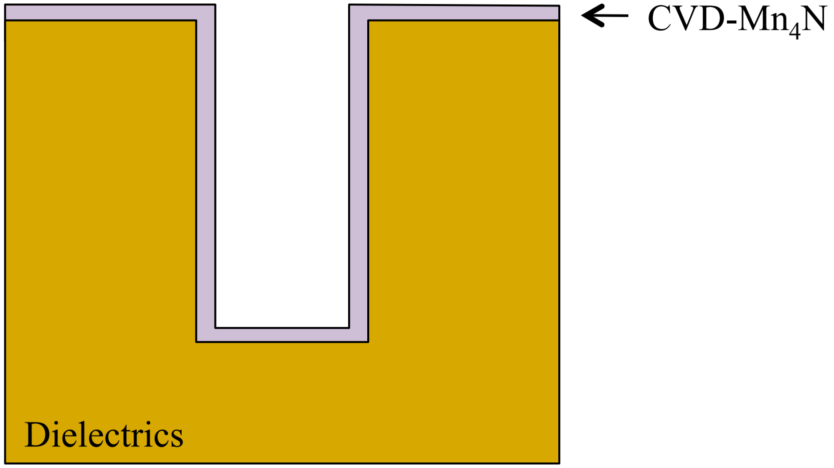
Surfactant Catalyzed Bottom-up Filling of CVD-Cu

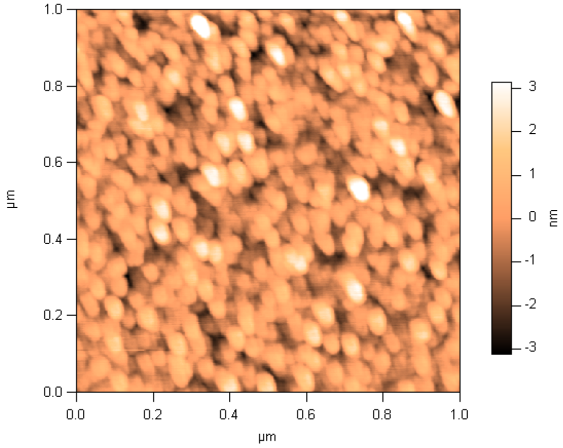
- CVD-Cu can be prepared by reacting copper amidinate precursors with H_2
- Presence of iodine surfactant catalyst promotes higher (10x) deposition rate and smoother surface morphology
- Iodine is not incorporated into the film



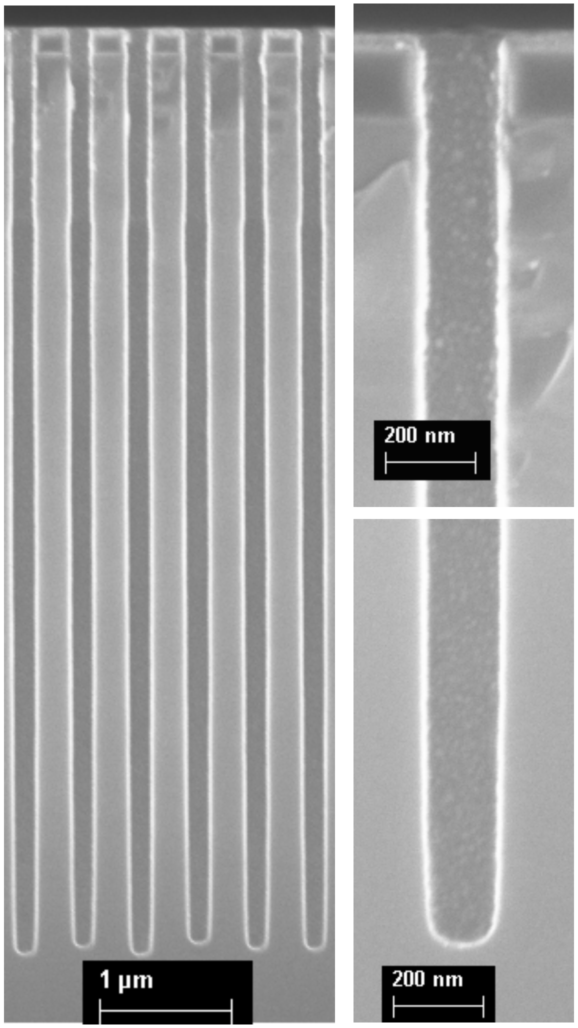
CVD-Mn_4N Barrier/Adhesion Layer

- CVD-Mn_4N (ε phase, FCC structure) can be prepared by reacting manganese amidinate precursors with NH_3





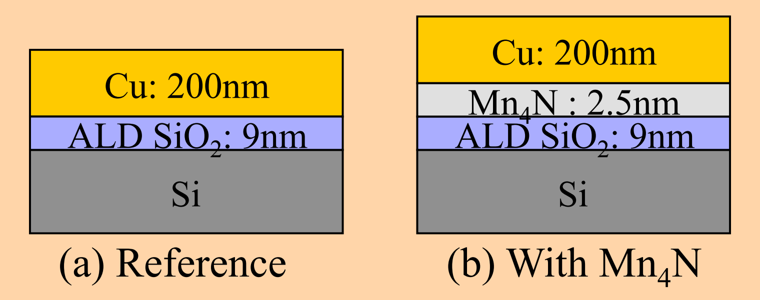
RMS roughness = 0.97 nm for a 13.5 nm film



Excellent step coverage holes with AR = 52:1

CVD-Mn_4N Barrier/Adhesion Layer

- Mn_4N layer as thin as 2.5 nm can significantly improve adhesion (debonding energy = 6.5 J/m^2) between Cu and SiO_2
- CVD Cu-Mn followed by anneal increases debonding energy to over 14 J/m^2
- Thin Mn_4N layer also shows barrier properties against Cu diffusion

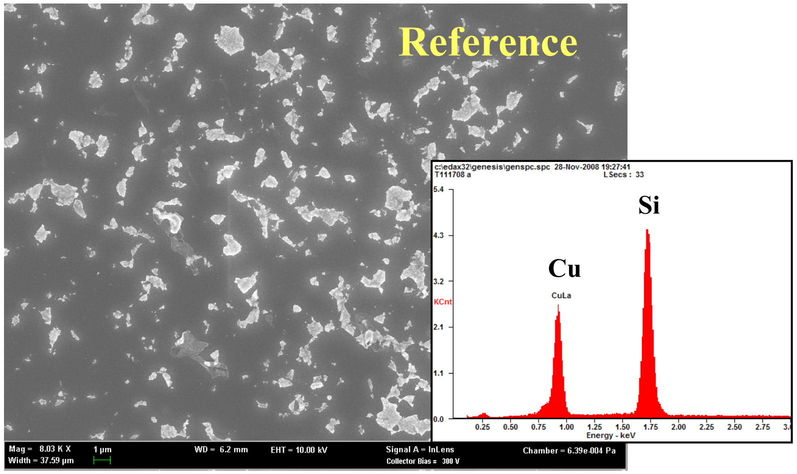


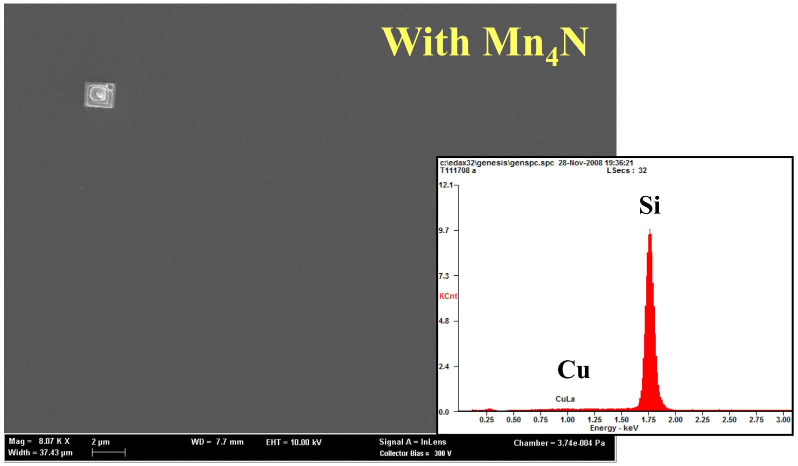
Cu: 200nm
ALD SiO_2: 9nm
Si

(a) Reference

Cu: 200nm
Mn_4N : 2.5nm
ALD SiO_2: 9nm
Si

(b) With Mn_4N





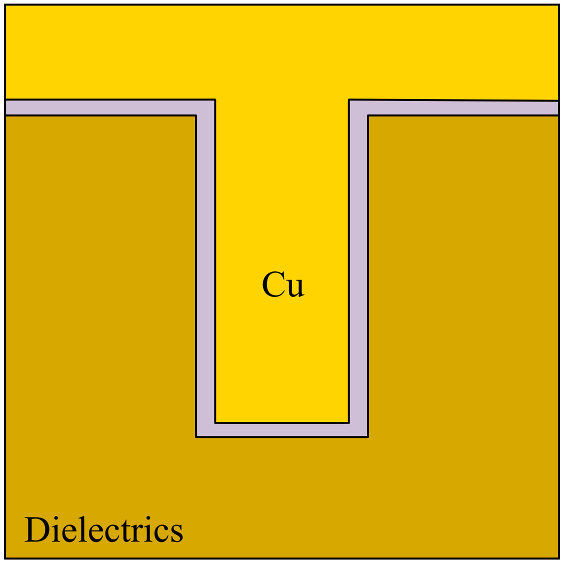
- Segregation of iodine and catalytic effects are observed on Mn_4N underlayer

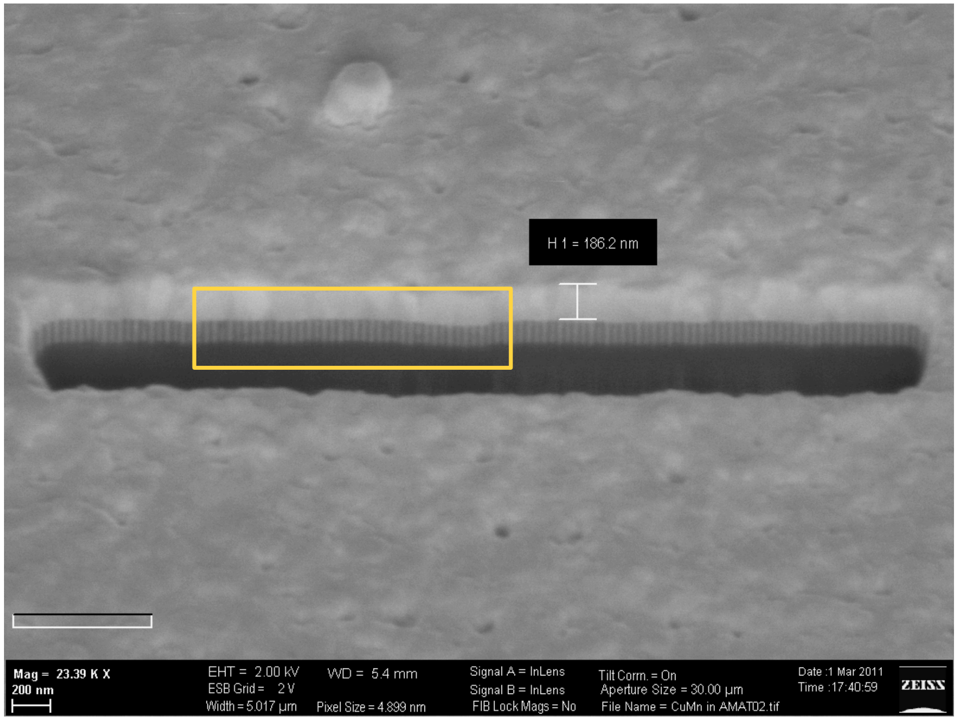
Surfactant Catalyzed Bottom-up Filling of CVD-Cu

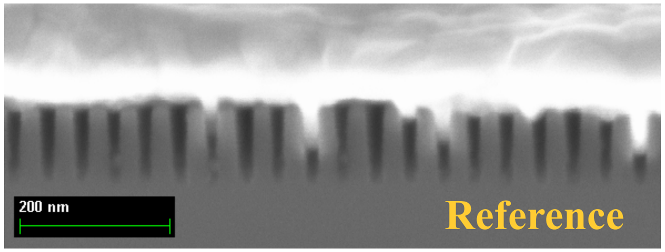
CVD-Mn_4N Deposition (130°C)

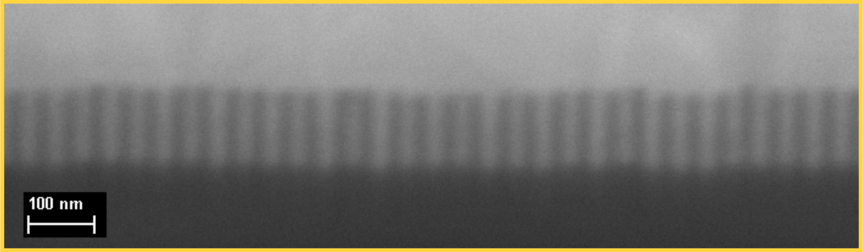
Iodine Exposure (RT)

CVD-Cu Deposition (180°C)





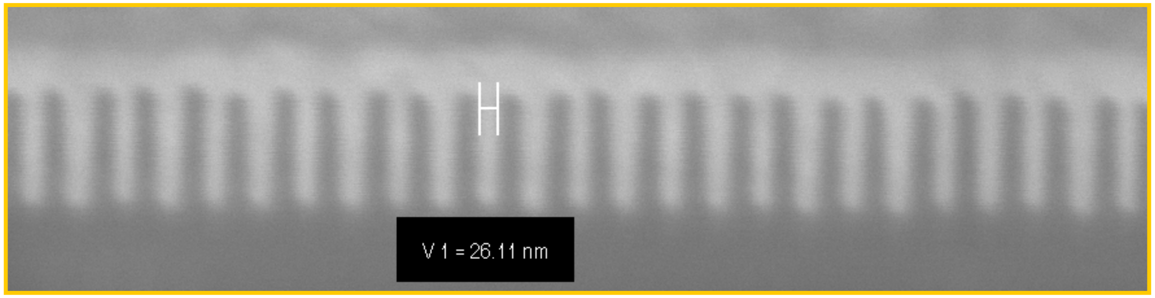




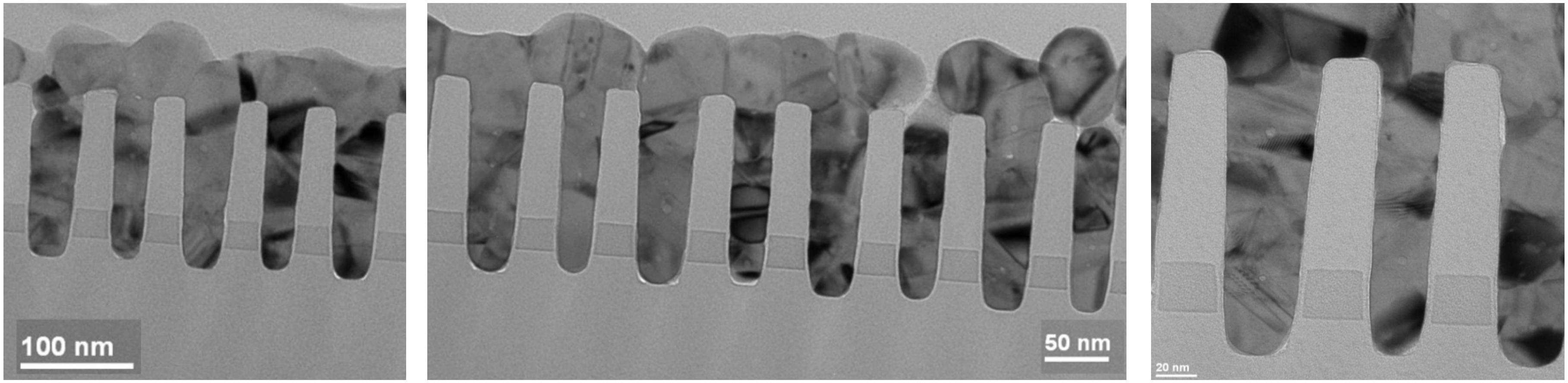
Surfactant Catalyzed Bottom-up Filling of CVD-Cu

CVD-Mn_4N Deposition (130°C) → Iodine Exposure (RT) → CVD-Cu Deposition (180°C)

SEM



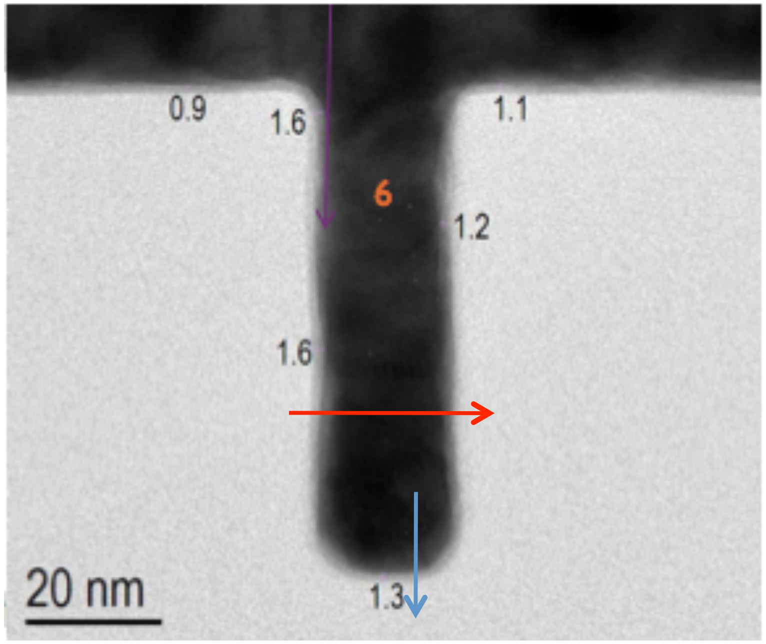
TEM



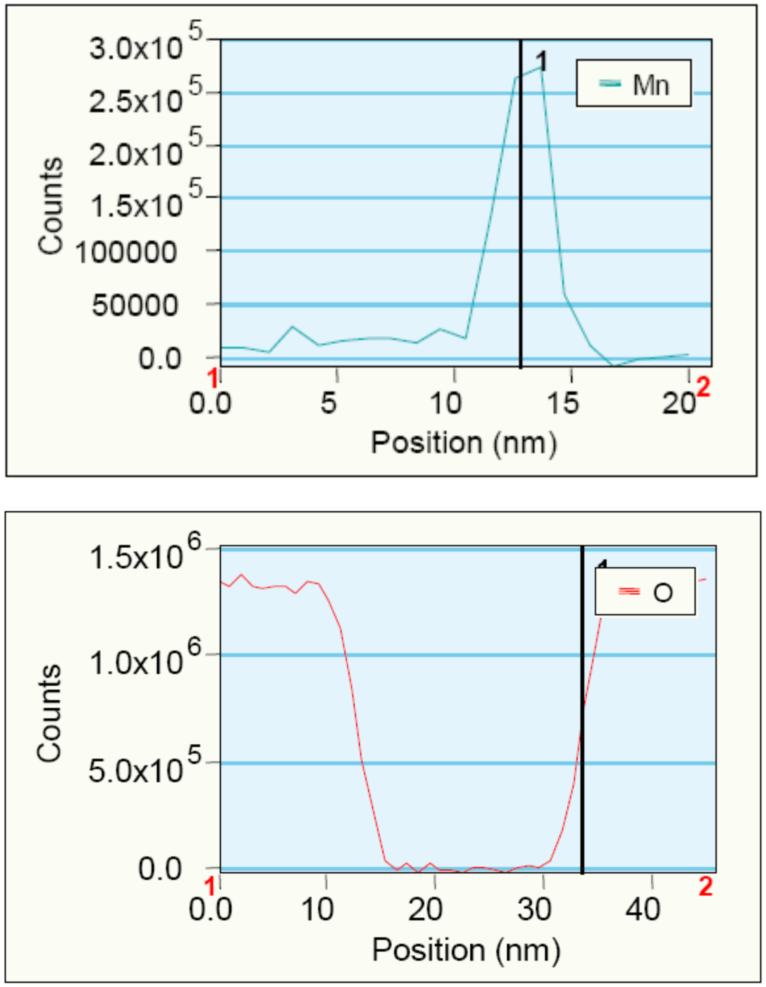
With CVD-Mn_4N liner layer and iodine catalyst, trenches with width ≤ 30 nm and aspect ratio over 5:1 can be completely filled with CVD-Cu

Surfactant Catalyzed Bottom-up Filling of CVD-Cu

18 nm Structure



EELS



- TEM confirms super-filling in sub-20 nm trenches
- EELS detects Mn barrier in the bottom of the trench and no oxygen contents in Cu film

Substrate, images and data courtesy of IMEC

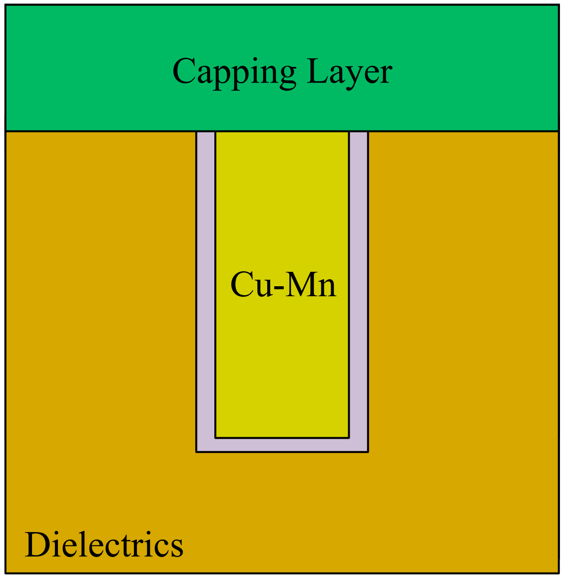
Surfactant Catalyzed Bottom-up Filling of CVD-CuMn Alloy

- Cu-Mn alloy can be formed by (1) alternating CVD-Cu and Mn or (2) co-depositing Cu and Mn

CVD-Mn_4N Deposition (130°C)

Iodine Exposure (RT)

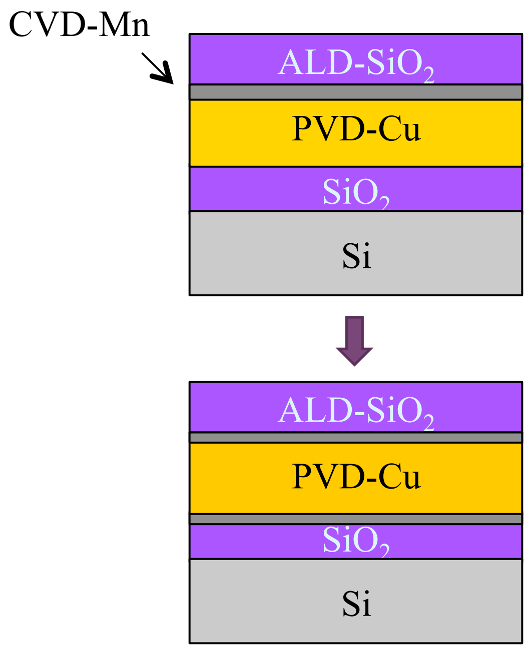
CVD-Cu & Mn (180°C)

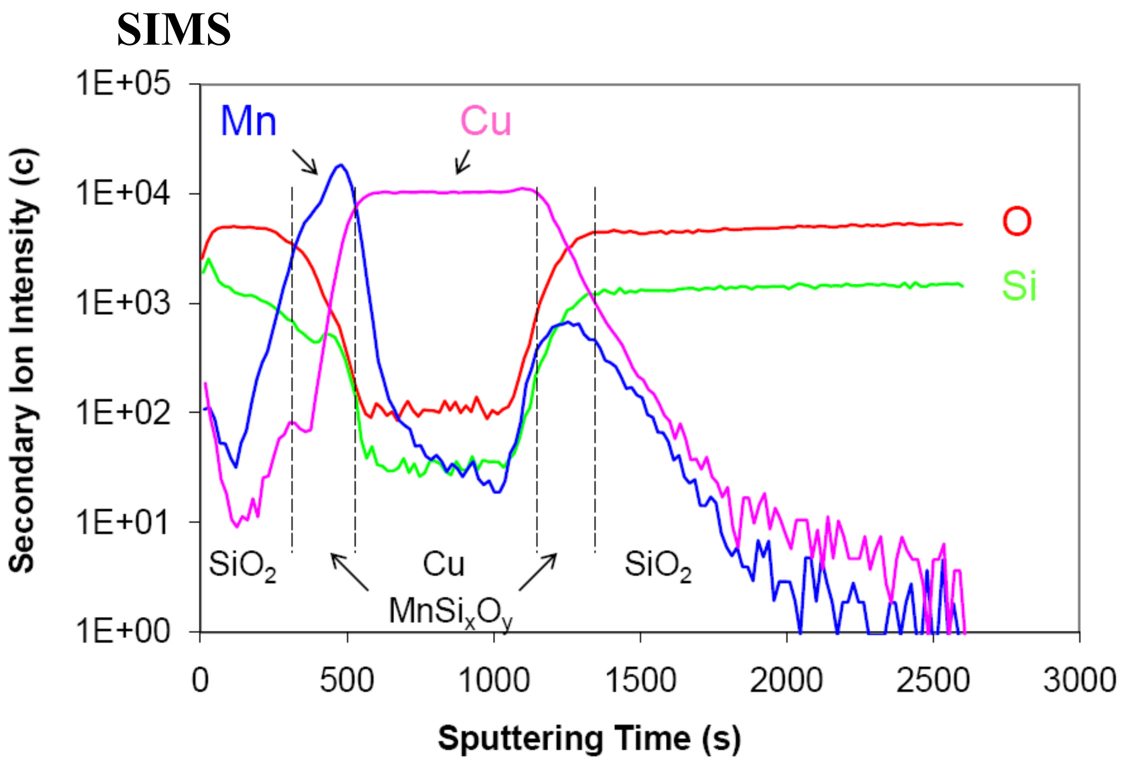


- Deposited Cu has a manganese concentration of approximately 0.5-2.0%

Diffusion of Mn in Polycrystalline Cu

- Insulators (SiO_2 and Si_3N_4) encourages diffusion of Mn through Cu grain boundaries to interface



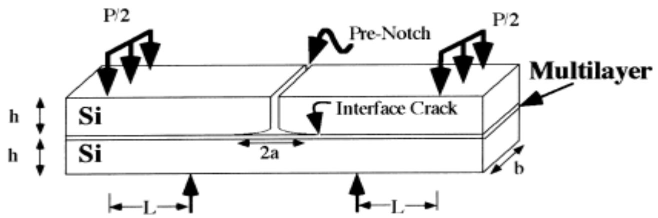

SIMS

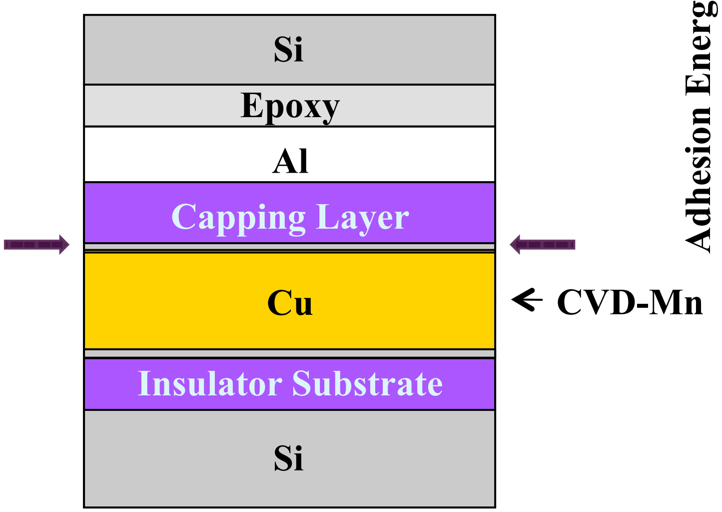
- XPS depth-profiling: **D ≈ $3x10^{-21}$ m^2/s** at 300°C
- CVD-CuMn process does not increase the resistivity of copper

Y. Au, Y. Lin, H. Kim, E. Beh, Y. Liu and R.G. Gordon, "Selective Chemical Vapor Deposition of Manganese Self-Aligned Capping Layer for Cu Interconnections", *J. Electrochem. Soc.*, **157** (6) D341-D345 (2010).

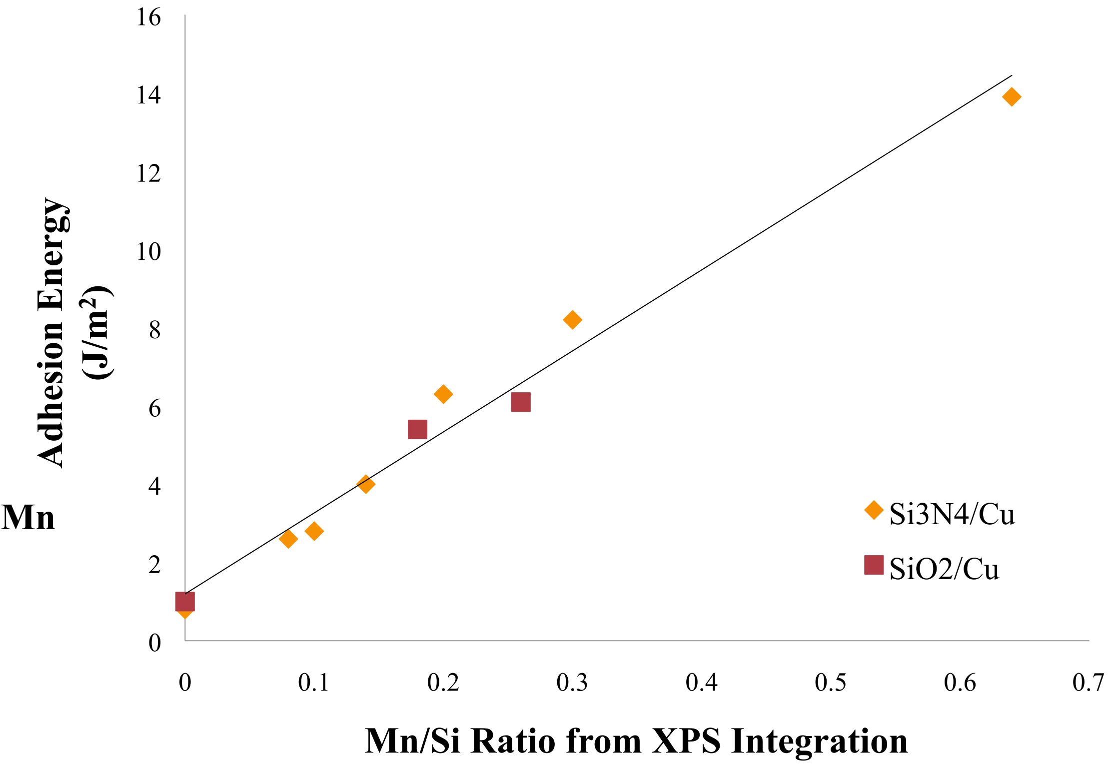
Adhesion Enhancement at Cu/Insulator Layer Interface

- Four-point bend technique evaluates adhesion enhancement at Cu/insulator interfaces





Adhesion Test Structure

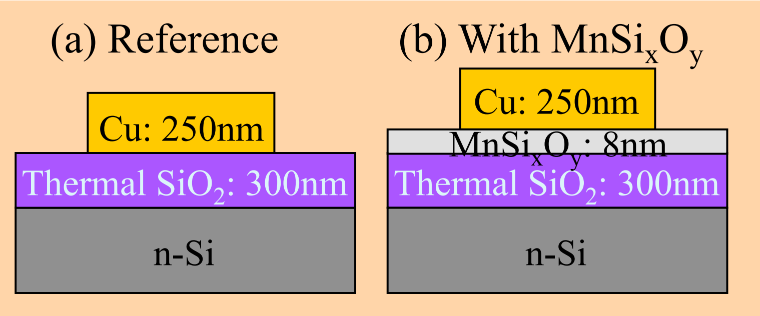


Debonding energy at Cu/dielectric interface increases linearly with the amount of manganese at the interface

Manganese Silicate Diffusion Barrier

- $MnSi_xO_y$ layer formed at the interface is an excellent barrier against diffusion of Cu, H_2O and O_2

Cu Diffusion Barrier Test



(a) Reference

Cu: 250nm

Thermal SiO_2: 300nm

n-Si

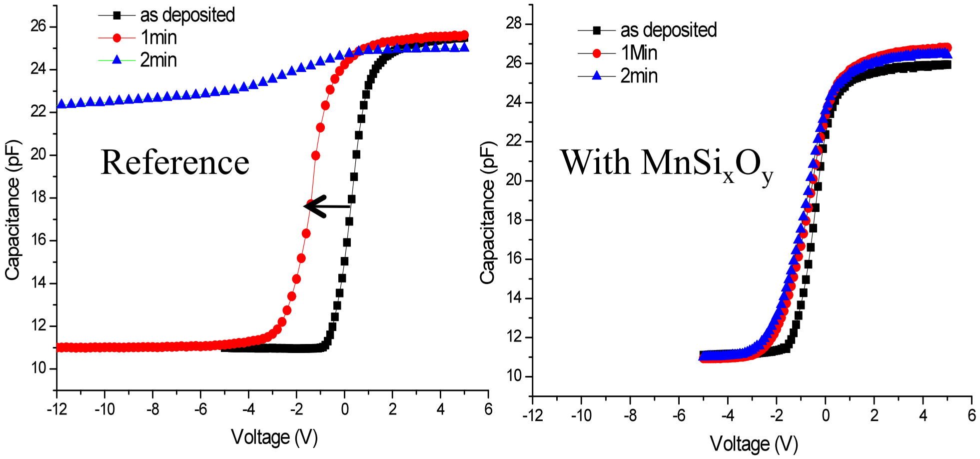
(b) With $MnSi_xO_y$

Cu: 250nm

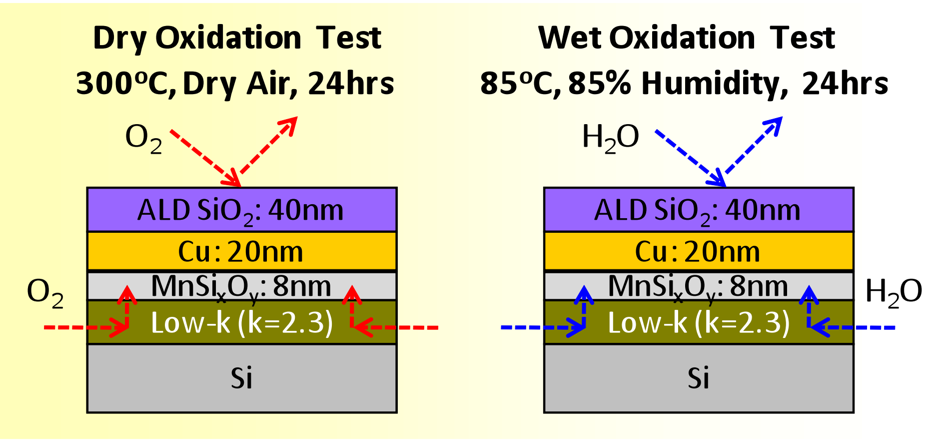
$MnSi_xO_y$: 8nm

Thermal SiO_2: 300nm

n-Si



Oxidation Barrier Test



Dry Oxidation Test

300°C, Dry Air, 24hrs

O_2

ALD SiO_2: 40nm

Cu: 20nm

$MnSi_xO_y$: 8nm

Low-k (k=2.3)

Si

O_2

Wet Oxidation Test

85°C, 85% Humidity, 24hrs

H_2O

ALD SiO_2: 40nm

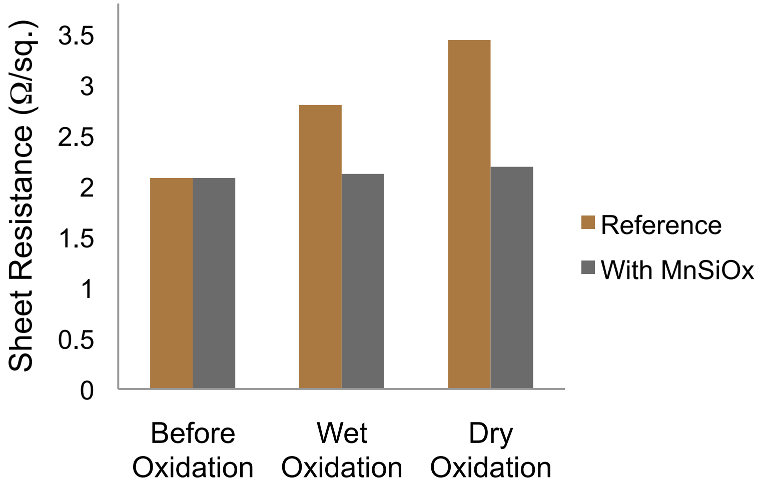
Cu: 20nm

$MnSi_xO_y$: 8nm

Low-k (k=2.3)

Si

H_2O



R. G. Gordon, H. Kim, Y. Au, H. Wang, H. B. Bhandari, Y. Liu, D. K. Lee, and Y. Lin, "Chemical vapor deposition of manganese self-aligned diffusion barriers for Cu interocnnections in microelectronics," *Adv. Met. Conf. 2008, Proc.*, p. 321 (2008).

Summary

- ✓ Copper and manganese can be deposited by CVD using metal amidinate precursors
- ✓ Nanoscale trenches can be superconformally filled by CVD-Cu and CVD-CuMn alloy with an iodine surfactant on Mn_4N liner layer
- ✓ Manganese in Cu-Mn alloy diffuses out to strengthen the interface between Cu and insulators without increasing the resistivity of Cu
- ✓ Manganese silicate ($MnSi_xO_y$) interfacial layer shows excellent barrier properties against Cu diffusion and protects Cu from corrosion by H_2O and O_2

Acknowledgements

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Harvard University
Center for Nanoscale Systems

- Precursors: Dow Chemical Company
  Substrates and Analyses: Applied Materials, IMEC and IBM

DOW APPLIED MATERIALS imec IBM

- Members of Gordon Group